HIGH Q INDUCTORS ON ULTRA THIN ORGANIC SUBSTRATES

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by

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HIGH Q INDUCTORS ON ULTRA THIN ORGANIC SUBSTRATES

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DEDICATION

To my mother, Mrs. Malathi Swaminathan for inculcating in me the spirit to fight, no matter what
and
to my grandparents, Mr. Swaminathan and Mrs. Rajam Swaminathan for giving me so much love and affection

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I wish to thank the Almighty for His love and blessings and for giving me the courage and determination to face every challenge with the right attitude.

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SUMMARY

Small size and cost reduction make the system on package approach an effective solution to RF front end packages. SOP provides functionality in the package through the integration of passives such as inductors, capacitors and resistors .One of the key technologies for higher integration in SOP's is embedded passives technology. High Q passives embedded in the substrate enable high performance with compact size. Such embedding of passives has been demonstrated in LTCC, multi chip module –D (MCM – D) technology. High Q passives have also been demonstrated on Liquid Crystal Polymer substrates. This thesis presents the design, fabrication and measurement of inductors on a new family of ultra thin organic substrates, thereby paving the way for further miniaturization in RF front end modules.

One of the chief components in a RF/microwave circuit is the inductor. The performance of the inductor affects the performance of widely used circuits such as the voltage controlled oscillator (VCO), low noise amplifier, and filter in the RF front end. It is very important to design inductors for accurate values of inductances and sufficiently high quality factors for these microwave applications. A key challenge in achieving high unloaded Q for an inductor in a thin substrate is the ground separation. This thesis aims at addressing this issue and achieving high unloaded Q's in the range 150 - 200 for a ground separation of about 100 - 140 microns in the frequency range of 1 - 15 GHz. One port and inductors will be designed using Electromagnetic field solvers. Various topologies will be explored for 2D and 3D inductors with the aim of achieving the desired inductance density and Q parameters in a minimum area possible. In order to address the issue of ground separation, design modifications will include the use of patterned grounds to take

advantage of the reduced parasitic capacitive coupling which enables a high Q factor. The objective of the thesis also includes demonstration of the usefulness of these high quality inductors in RF front ends. To this effect, proof of concept designs of LC band pass filters will be presented. To enable this design, capacitors will also be designed. An extensive library of the designed inductors will be presented as a part of the thesis.

The designed components will be fabricated at the Packaging Research Center (PRC), Georgia Tech using organic substrate compatible processes. High frequency measurements will be made with the Vector Network Analyzer (VNA) along with suitable de - embedding to demonstrate the correlation between designed and fabricated results. Following this, circuit models will be built for the characterized inductors.

CHAPTER 1

INTRODUCTION

Electronics manufacturers are squeezing greater functionality into smaller, more portable products, and the number of passive devices required for these products has increased significantly. For example, the typical Pentium III motherboard uses approximately 2,200 passive devices. Another example are the, 500 passive devices on the printed circuit board (PCB) of a typical cell phone . The growing number and types of passives used in PC motherboards are listed in Table 1.1 [1] . Designers have several choices for accomplishing the passive functions: discrete passives, array passives, passive networks, integrated passive devices and embedded passives. Table 1.2 gives a summary of the influence of these types of passives on system performance. In addition to these components, designers may also select on-chip passives, where the passive elements are fabricated along with the active elements as part of the semiconductor wafer.

Table 1.1 Types and number of passives used in PC motherboards

Motherboard:	486	Pentium 120	Pentium 200 MMX	Pentium II 333 MHz	Pentium III
Leaded MLC	58	0	0	0	0
Surface Mounted MLC	0	151	190	300	600
Cap Arrays (4)	0	0	32	140	200
Leaded Tantalum	15	1	0	0	0
Surface Mounted Tantalum	0	0	0	37	80
Aluminum	0	7	32	11	15
Feedthrough	0	0	3	0	0
Disks	0	0	0	4	0
Leaded Resistors	92	0	0	0	0
Surface Mounted Resistors	0	146	188	635	1,000
Resistor Arrays (x2)	0	0	0	10	0
Resistor Arrays (x4)	0	64	148	336	300
Total	165	369	593	1,473	2,195

Table 1.2 Influence of passives on system performance

Parameter	**Discretes**	**Arrays and Networks**	**Integrated Passive Devices**	**Embedded Passives**
Definition	A single passive element in a leaded or packaged case	Passive arrays combine multiple passive elements of similar function	Multiple passive devices of more than one function and maybe actives as well	Passives are buried in the substrate material
Cost	Good	Suitable for local densities of four or eight devices packed together	Suitable for application specific high local densities	Cost is panel size dependent
Size	Sufficient board area is required for each and every device	More than 50 % board area saving is possible	Application specific IPD's can replace dozens of components	Best because no surface area is required
Performance	Self resonates at low frequencies	Self resonates at low frequencies	Qualified to several GHz	Best because of the absence of inductance due to the connections loops and and decreased lead lengths
Reliability	Heavy use of solder joints	Reduced use of solder joints	Better than array passives	Elimination of solder joints

Embedded passives are buried (embedded or integrated) into the substrate material. The substrate might be of ceramic, FR-4 board or a small laminate package substrate. As long as the passive elements are an integral part of the substrate, they are called embedded or integral passives; but not to be confused with *integrated* passive devices (IPDs). The deciding characteristic is that the passive component does not need to be mounted on or connected to the substrate. It is distinguished from the "super component" (IPD) because it acts as the system board.

The trend in wireless systems is toward higher miniaturization and multi-functionality at higher speeds and lower cost. System-on-chip (SOC), system-in package (SIP), and multiple-chip-module (MCM) are the platforms that are currently being widely pursued by industry to accommodate such challenging tasks. Even though complementary metal–oxide–semiconductor (CMOS) technology can be the most cost-effective solution for certain digital and RF applications, it is not an optimal technology for entire RF and digital applications. As the number of components in a multi-band system has increased exponentially, as shown in Figure 1.1 ,[2] new system integration platforms such as SOC and SOP are critical.

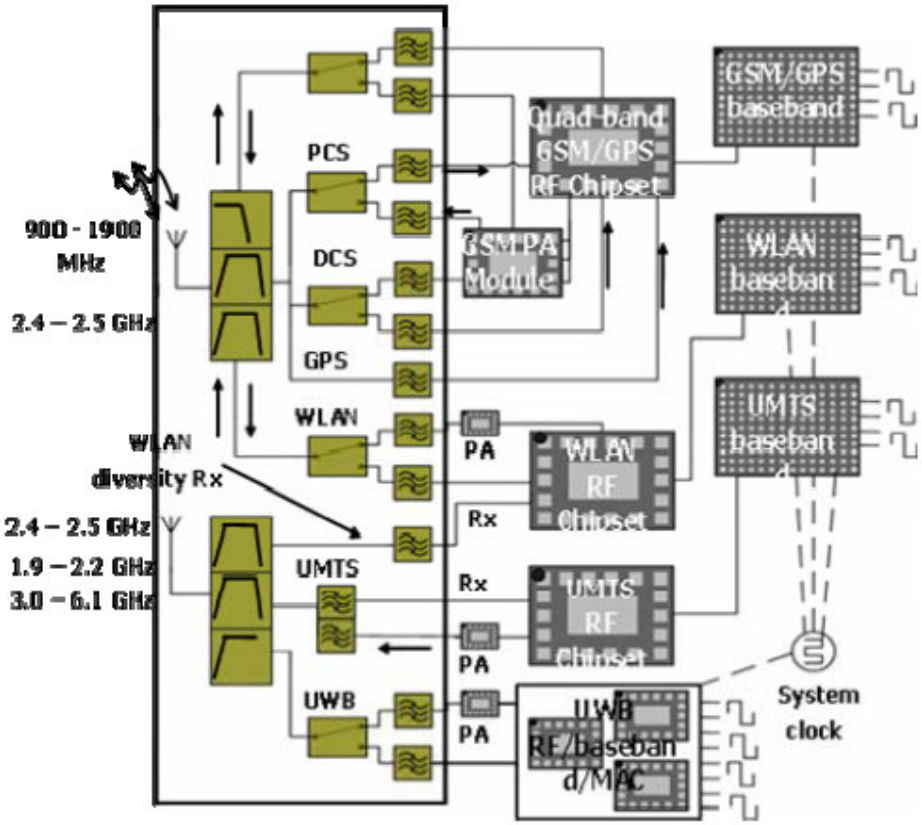


Figure 1.1 Multiband System

1.1 SOP and SOC for passives

SOC is a method to integrate certain CMOS-compatible components using CMOS process technologies. It can achieve very high density of components, however, it has certain limitations, such as low-Q , substrate coupling, and testing. Using SOC alone, it is difficult to realize filters, duplexers, power amplifiers, and antennas. If they can be achieved, they are not optimal for properties, size and cost. In addition, the nano-scale integration trend increases wiring resistance, leading to delay, causing increased latency in digital circuits. The SOP technology, however, combines the best of on-chip integration with the best of package integration for convergent and microminiaturized

mobile systems. The SOP concept overcomes a number of the engineering limits of SOC. To reduce the electrical delay or latency in SOC technology, SOP can provide global wiring on the package by means of lower resistance wiring. The wireless integration limits of SOC are also handled effectively through SOP. Figure 2.2 shows the state-of-the art mixed-signal SOP technology. RF components such as capacitors, filters, antennas, switches, and high-frequency and high-Q inductors are best fabricated in the package rather than on silicon. The highest Q factors of inductors reported on silicon are about 10-25, in contrast to 100-400 achieved in the SOP package. SOP has proven that it is an effective system with low cost, high performance, and small form factor [3], [4], [5], [6], [7], [8], and [9]. As shown in Figure 1.2, the high-Q embedded passive serves not only as RF components, including filters, BALUNS, and antennas, but also as low parasitic and low insertion loss interconnects using high-Q passives in the substrate.

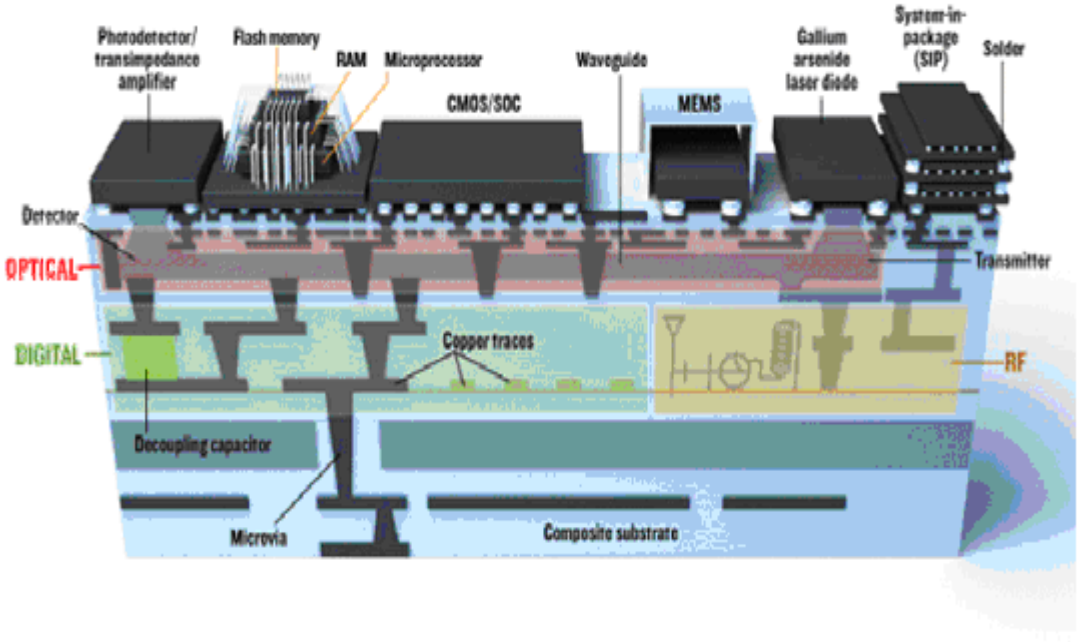


Figure 1.2 State of the art Mixed Signal SOP

1.2 Passives in RF Packaging

In the domain of RF packaging , the common constituents of the packages are filters (lumped and distributed), couplers, RF crossings, impedance matching networks and antennas. Passives (R, L and C) applications in RF include

- Signal inductors (1 – 20 nH)
- Signal capacitors (1 – 20 pF)
- Decoupling capacitors (0.01 – 0.1 uF)
- Choke inductors (1 – 10 uH)
- Terminating resistors (20 – 100 ohms)
- Signal resistors (10 – 100 ohms)

1.2.1 Discrete and Embedded Passives

At very high frequencies (eg: RF), the physical dimensions of discrete components becomes a considerable portion of the signal wavelength (normally one – tenth to one – fifth). This makes the surface mount components unsuitable for these applications. This problem can be overcome by using embedded and thin film passives where the overall and the pad dimensions can be made smaller resulting in a smaller form factor. Such small form factors can be implemented on the silicon surface resulting in all- RF functions being accommodated in a single ASIC. However, the large value of the L and C's required increases the area occupied on the silicon, thereby raising the cost of the die. Also, with larger values are the associated larger parasitics. These are some of the hindrances to the growth of RF systems for low cost applications.

As a remedy, passives can be embedded into a multilayer organic package or board as shown in figure 1.3

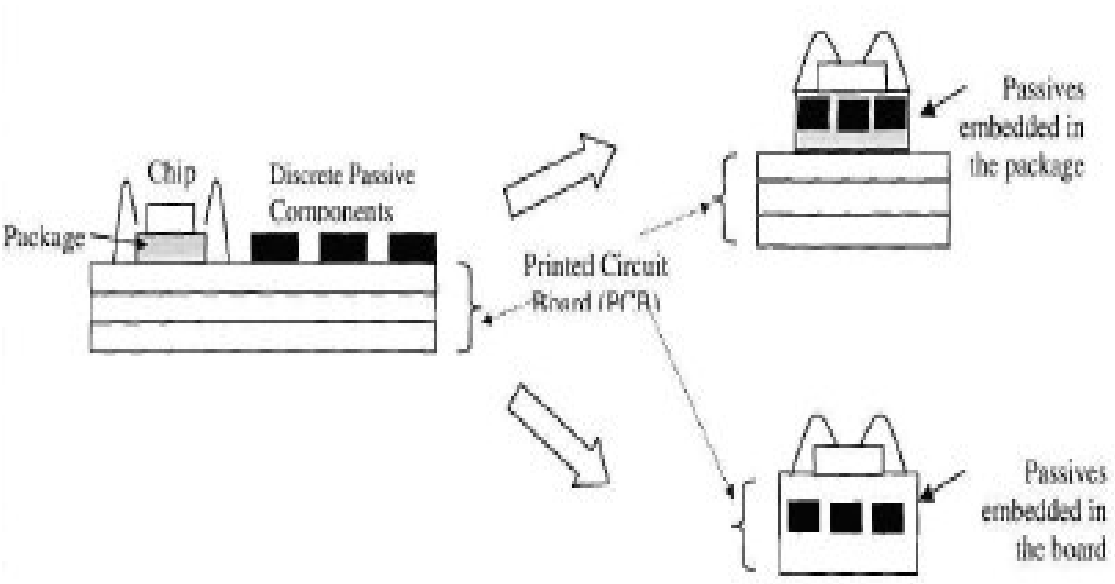


Figure 1.3 Discrete and Embedded Passives

With current advancements in fine-line and microvia packaging technologies, many critical passive components can be made to occupy a small area of the package substrate. Shifting passive circuit elements from the die to the package reduces the die size and cost, and improves crucial performance metrics such as the phase noise of voltage-controlled oscillators (VCOs). The phase noise of a VCO is inversely proportional to the square of the quality factor. Technologies that enable the integration of passive components therefore have a potential for the:

- Reduction in circuit board area and weight
- Increase in functionality for a given product size
- Increase in the manufacturing throughput
- Reduction in the inventory and improvement of product reliability
- Reduction in the functional block and system level costs

- Enhanced design ease by eliminating the problems associated with lead and pad parasitics, matched impedances, higher tolerances for devices and reduction in the number of packaging style variants

1.2.2 Embedded Inductors

An RF system consist of a large number of inductors and the feasibility of realizing appropriate value of inductances with high quality factor and occupying a small area is one of the major challenges. The performance of the inductor affects the performance of widely used circuits such as the voltage controlled oscillator (VCO), low noise amplifier, and filter in the RF front end. It is very important to design inductors for accurate values of inductances and sufficiently high quality factors for these microwave applications. The Figures of merit associated with RF inductor design are the effective inductance, quality factor and self resonant frequency. These parameters provide a good evaluation of the designed inductor.

1.2.3 Challenges in high Q inductors

The integration of high quality factor inductors has been a perennial challenge in the domain of RF module design. The key to understanding the nuances of the design flow of these RF inductors lies in understanding the fundamental limits that affect the Quality factor of these structures and hence the performance. This section explains the critical parameters that affect the performance of these structures.

A central problem in highly integrated RF modules is the conflict between achievable Q and electrical isolation.[10].Considering the simple microwave cavity as shown in the figure 1.4 .The inductance, capacitance and resistance per unit length are limited by the following expressions.

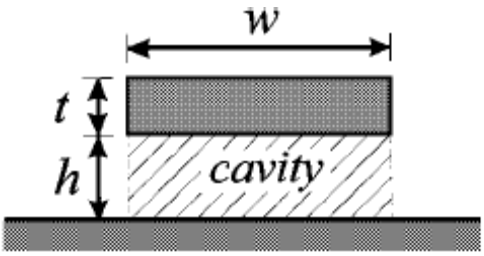


Fig 1.4 A typical microstrip cavity

$$C_0 > \varepsilon w/h. \tag{1.1}$$

$$L_0 < \mu h/w. \tag{1.2}$$

$$R_0 = \rho/(wt) \tag{1.3}$$

where ro is the resistivity of the metal. From the above equations the quality factor is given by the expression

$$Q \equiv \omega L_0/R_0 < \omega \mu h t/\rho \tag{1.4}$$

where omega is the angular frequency. It is sensible to introduce the skin depth in these expressions and hence the quality factor at low frequencies is given by

$$Q < \frac{\mu}{\mu_C}\left(\frac{2ht}{\delta^2}\right) \tag{1.5}$$

And at high frequencies it is given by

$$Q < \frac{\mu}{\mu_C}\left(\frac{4h}{\delta}\right) \tag{1.6}$$

In a nutshell, observing the above expressions closely, the performance of the inductor or any transmission line is primarily dependent on the following factors

1) *Distance from the ground* : The quality factor increases with increased ground separation
2) *Thickness of the conductors*: Thicker conductors give higher quality factors.
3) *Resistivity of the conductor*: Conductors with lower resistivity give higher Q's.

Apart from these factors, there are certain loss mechanisms that arise from the substrate and the metallization.

1) *Metal losses* – Inductors make use of at least two metallization layers. At frequencies lower than the frequency of the maximum quality factor ,the quality if the inductor is determined by the conductivity if the metal tracks since the current flow produces ohmic losses. At higher frequencies, the distribution of the currents is non- uniform due to the skin and proximity effects. As the frequency continues to increase, the effective area available for current circulation reduces and therefore there are losses due to the Joule effect.
2) *Substrate losses* – The conductive nature of the substrate causes several loss mechanisms
    a. Electrical coupling between the various metal layers within the substrate due the presence of dielectric.
    b. Currents induced in the substrate due to the variable magnetic fields.

1.2.4 Literature Search

The integration of RF front end modules has been a key driver for the development of next generation wireless communication systems. These portable and low power applications require a very high level of integration, high performance devices and low

manufacturing techniques. An important component of these high performance RF modules are inductors, which form a critical part in the design of filters, voltage controlled oscillators, power amplifiers, low noise amplifiers etc. The figures of merit when dealing with inductor performance are

- Inductance (L)
- Self Resonant Frequency (SRF)
- Quality factor (Q)

This section gives an overview of the research reported inductors so far. Inductors can be broadly classified based on the type of substrates they are fabricated on namely

- Silicon
- Ceramic
- Organic.

1.2.5.1 Inductors on Silicon

Many approaches have been reported to achieve high Q on Silicon .Some of them use high resistive silicon substrates, thick dielectric layers and/or thick conductor lines , multilayer conductors and also micromachining techniques.

Single and double level inductors have been fabricated on silicon [11].The silicon substrate used for the single and double level inductor is shown in figure 1.5.

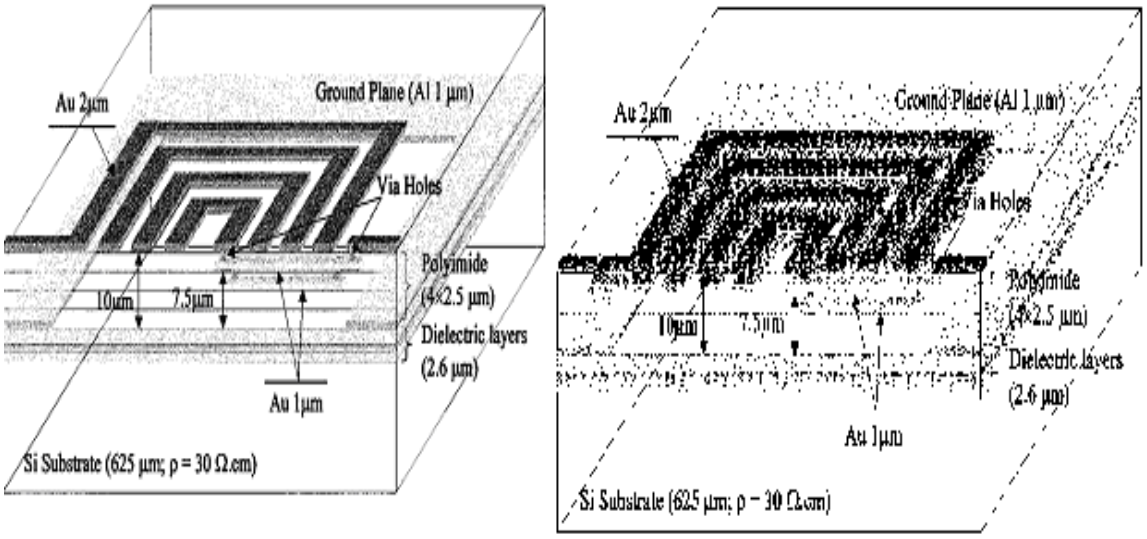


Figure 1.5 Silicon substrate

A 3D process was implemented in single layer and multilayer spiral inductor.It was observed that the inductance observed in the case of a single layer inductor was higher when compared to that of a double layer inductor. For a line width of 20 um ,a spacing of 5 um , substrate thickness of 625 um, a quality factor of 52.8 was observed at a frequency of 13.6GHz and a SRF of 24.7GHz.

A high speed complementary bipolar process has been used to build inductors with Q of over 12 for use in wireless applications. [12].16 square inductors were built on a test array of outer dimensions of 300um.A spacing of 4 um was used on each inductor. An oxidized porous silicon layer of 25 microns thickness was used on a SiO2 substrate to obtain a high performance planar inductor [13] as shown in the figure 1.6.

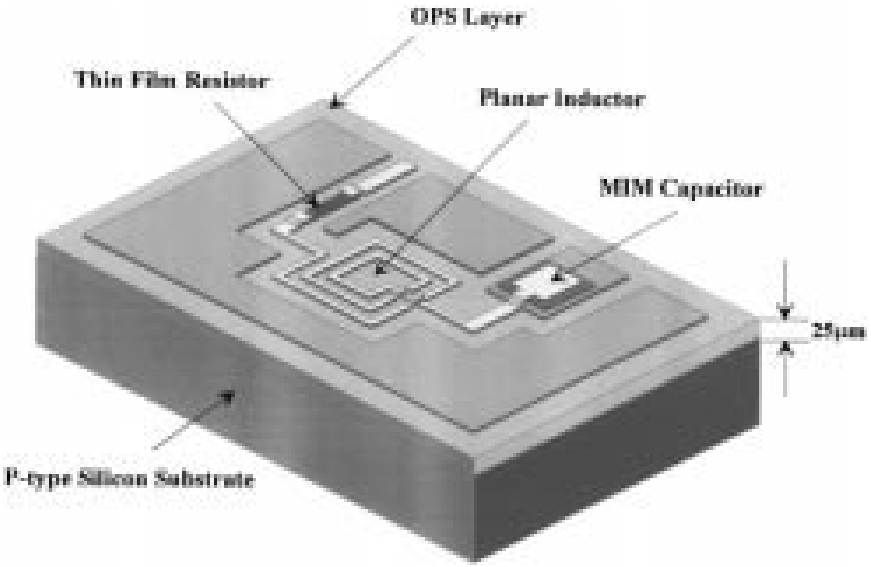


Figure 1.6 Silicon substrate with oxidized porous silicon layer

A Q of 13.3 was obtained for a 6.29nH inductor with a self resonant frequency of 13.8GHz.Instead of direct oxidization of bulk silicon, oxidation process of porous silicon was used to make the thick oxide layer. A quality factor of up to 30 and self resonant frequency higher than 10GHz was obtained when polysilion spiral inductors encapsulated with copper were suspended over 30 um deep cavities in the silicon substrate beneath[14].The metallization process simultaneously coated the inner surfaces of the cavities with copper to form a good radio frequency ground and an electromagnetic shield. The schematic of such a polysilicon inductor is shown in the figure 1.7

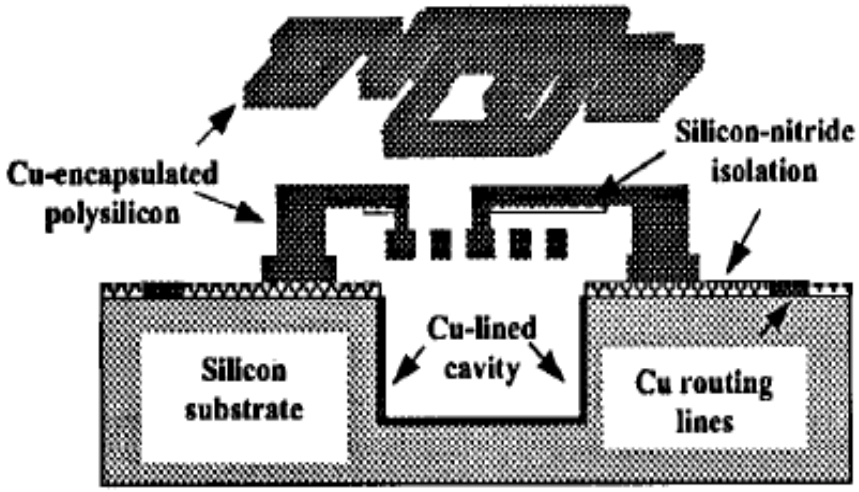


Figure 1.7 Polysilicon inductor

To achieve cost and size reduction, a low cost manufacturing technology for RF inductors was developed by utilizing a passive integration process using copper metallization and BCB interlayer[.15].A 10um copper plating process for low loss inductor fabrication and interconnection was used. The fabricated inductor library showed the maximum quality factor in the range of 30-120 and inductance values in the range of 0.35nH – 31.5nH around 4GHz.

1.2.5.2 Wafer Level Packaged Inductors

Wafer level packaging refers to the technology of packaging at Silicon wafer level, instead of the traditional process of making an organic substrate and assembling the package of each individual unit after wafer dicing. WLP is a true chip scale packaging technology, since the resulting package is practically of the same size as the die. The

other aspects of WLP is that it provides for the integration of wafer fabrication, packaging, test and burn in at wafer level.

The wafer level packaging technology, when applied to the integration RF inductors on silicon substrates, produces good results with sufficient increase in the quality factor as compared to the other technologies

Inductors integrated in today's typical silicon processes do not meet the high performance specifications of the RF modules. The major shortcoming of the silicon substrate which results in low Q's is the lossy nature reflected by its very high loss tangent and the dielectric constant. Also, these processes use an Al-Cu metallization to pattern these and inductors and underpasses and due the highly dense integration levels, the metal thickness is typically thinned to achieve the desired pitch. Therefore, on chip RF inductors have low Q factors due to the relatively thin metal layers and close proximity to the lossy Silicon substrate. The inductor performance can be improved by using low K materials and thick copper traces, however this is not a back end of line process(BEOL).An attractive cost effective solution is to realize these inductors using wafer level packaging techniques.

In this technique, the on chip inductors are realized above the passivation layer using thin film post processing techniques. Such a process is shown in the figure 1.8. [16]The advantages of thin film technology are high precision, low temperature, and low cost. When applied above IC, this thin film wafer level packaging technology offers characteristics such as redistribution of bonding pads along with high quality factor achievement. In the figure 1.8, benzocyclobutene has been used to achieve high Q.

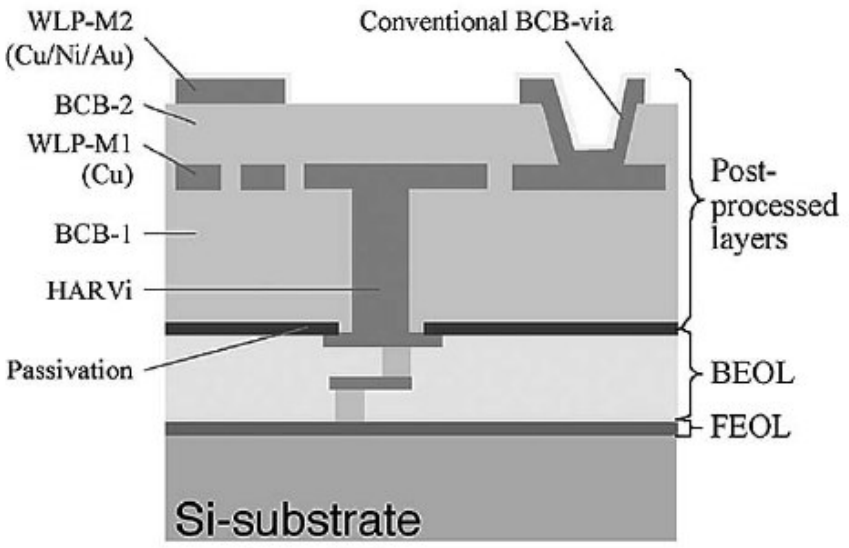


Fig 1.8 WLP technology for high Q inductors

1.2.5.3 Inductors on Organic Substrates

Some of the high performance inductors have been fabricated on LCP, which is an extremely attractive material as a high frequency circuit substrate and package material due to its ultralow loss and low dielectric constant over a wide high frequency range , near hermetic behavior as a result of superior moisture barrier properties, flex circuits and microvia laminates for high density interconnections. LCP has a loss tangent of 0.002 and a CTE of 8-17 ppm/K.

Inductors were fabricated on LCP [17], the test vehicle for which is shown in figure 1.9. Various designs that included the spiral with a 125 micron width were fabricated .A maximum Q in excess of 70 was obtained in the c band.

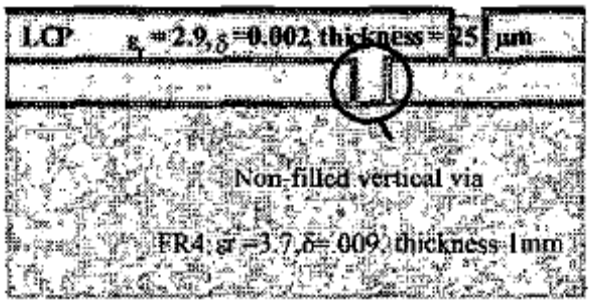


Figure 1.9 LCP substrate

Planar CPW loop inductors with a high Q of 85 in the 5GHz range were demonstrated on Nelco N4000-6 type material[18].The cross section showing the floating ground and the ground for the coplanar structures is shown in figure 1.10 .The results obtained are as shown in figure 1.11

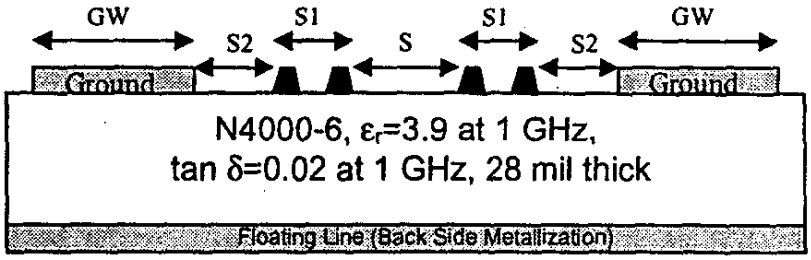


Figure 1.10 Nelco N4000-6 substrate

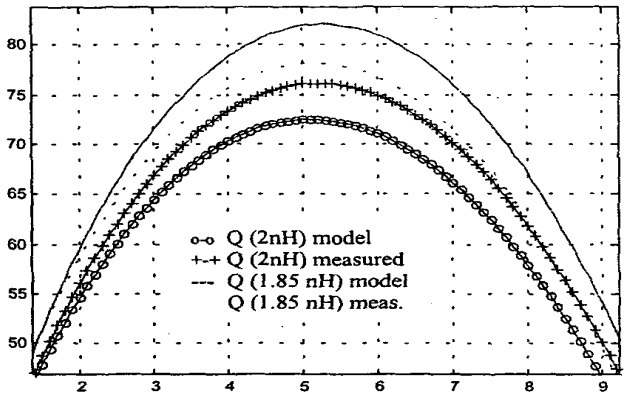


Figure 1.11 Results obtained for Q

A maximum Q of 100 was measured for a 3.6nH inductor at 1.8GHz on standard FR-4 substrate using a build up layer of DuPont vialux [19].The process used was a low cost large area MCM-L technology. The cross section of the test vehicle is as shown in figure 1.12

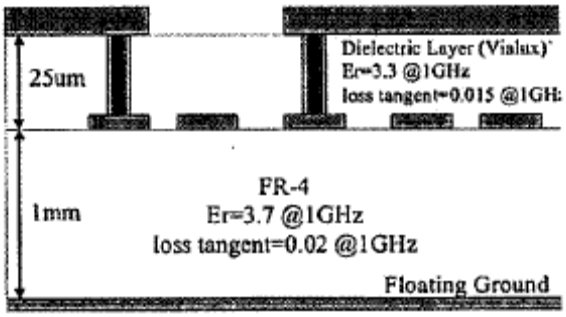


Figure 1.12 Dupont Vialux substrate

The self resonance frequency was 10.6GHz.About 150 variations of the inductor designs were built on this test bed and a variety of structures were experimented for variations in parameters such as line width, spacing, ground separation and the number of inductor turns. A Q of 103 was demonstrated for a 11nH inductor at 2.2GHz with a self resonant frequency of 3.6GHz[20].A unique design using cascaded loops was used as shown in figure 1.13

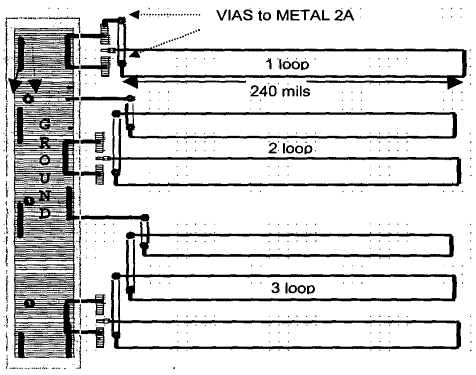


Figure 1.13 Loop Inductors

The cross section of the test bed used is shown in figure 1.14 .The substrate was FR4 with buildup layers of DuPont vialux.These inductors are microstrip designs and occupied an area of 240*21 mils^2.

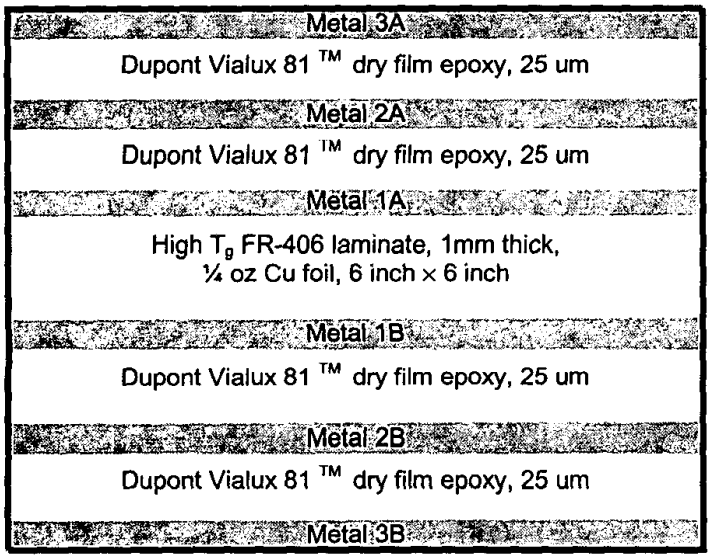


Figure 1.14 FR4 substrate with build up layers of Dupont Vialux

A high Q of 180 has been obtained in the frequency range of 1-3GHz for an inductance range of 1nH to 20nH[21].The cross section of the test bed is shown in the figure 1.15.

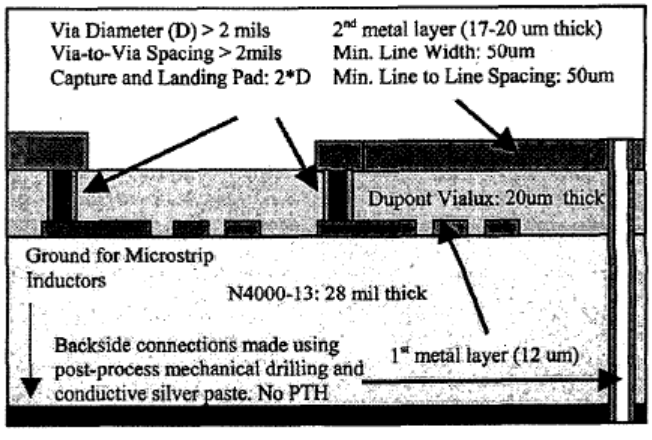


Figure 1.15 Nelco substrate

Microstrip loop, microstrip spiral and CPW loop inductors with hollow ground were designed. There was only one layer of DuPont vialux. This was done to minimize via registration and alignment problems. A Q of 110 was obtained for the microstrip loop inductor with a width of 6 mils and spacing of 4 mils A microstrip spiral inductor gave a Q of 170 at 2.4GHz with an area of 3.2mm2 and SRF of 8.5GHz.The highest Q of course, was for a CPW loop inductor with a Q of 180 at 2.2GHz and occupying an area of 9 mm2 with a SRF of 5.5GHz.

1.2.5.4 Inductors on Ceramic

A fully -embedded LTCC spiral inductor incorporating air cavity between the spiral and ground plane is used to achieve a quality factor of about 51 with a SRF of 9.1GHz.[22].The air cavity employed under the spiral reduces the shunt parasitic capacitance of the inductor, and results in high Q factor and high SRF of embedded inductors. The inductors were designed using a low loss LTCC dielectric of 114um thick per layer and silver conductor of 12 um thick. The spiral inductors with air cavity incorporated were fully embedded in a 5- layer LTCC block as well as those without air cavity. The cross section is shown in the figure1.16

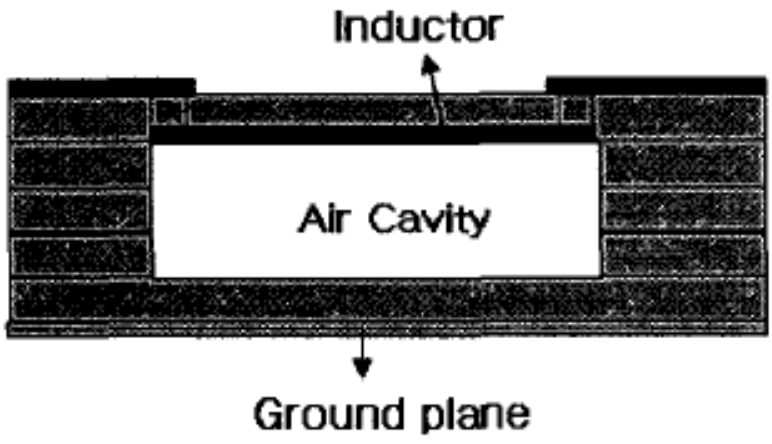


Figure 1.16 5 layer LTCC block

A quality factor of 93 at 1.1GHz and SRF of 3.11GHz was reported when 3D helical inductors with circular turns were designed on 20 layer LTCC-951-AT ceramic.[23].The 3D helical inductors occupied less space.An inductance of about 9.6nH was obtained. The helical inductor fabricated is shown in the figure 1.17. In addition to occupying less space, the helical configuration reduces the coupling capacitance by increasing the distance between the top turns and the underlying turns, thereby preventing considerable reduction in SRF.

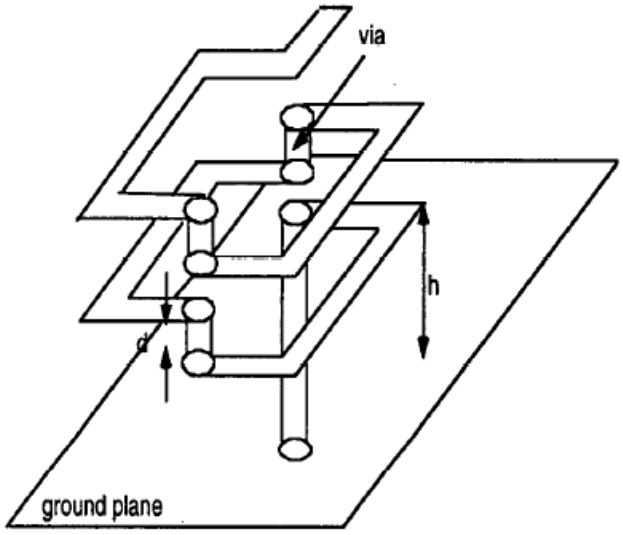


Figure 1.17 Helical Inductor

The Table 1.3 summarizes the highest Q achieved in the three technologies discussed thus far

Table 1.3 Summary of High Q inductors

	Quality Factor	**Inductance**	**Frequency**	**Distance to ground (um)**	**Area (mm^2)**
Silicon					
- On Chip	[11]52.8	1.38nH	13.6GHz	600	0.04
- High Resistivity	[24]30	4nH	1-2GHz	600	0.5
- Micromachined	[25]>150	1nH	8 – 23 GHz		
Wafer Level Package	[16] 38	1nH	4.7GHz		
LTCC	[23]93	9.6nH	1.15GHz	1800	2.25
Organic Laminate	[21]180	4.8nH	2.2GHz	800	4.3

As seen from the table, the typical separation to the ground plane in the case of organic substrates is about 800 – 1000 microns. This separation is critical in achieving high Q. Keeping this ground separation in mind, it is possible to state a new metric for the integration of inductors for RF applications – the volume density required for the inductors. The 2D integration (lateral area occupied) of these components has been done very efficiently in the technologies presented thus far. However, the vertical dimension required for efficient RF performance is still very high (of the order of 500 – 100 microns). Therefore, the aim of the current research is to achieve similar Q's in packages

of thickness of about an order smaller than the current laminates, thereby improving volume density for packaging these inductors. In this direction, there has also been an effort to minimize further the lateral area occupied by these structures to enable miniaturization in the true sense of the term.

1.3 Objectives of the research

Given the scenario and challenges in RF packaging and design of high Q inductors**,** the proposed research attempts to address the issues related to the design and fabrication of high Q embedded inductors of reduced form factor using ultra thin organic substrates. The objectives of the research are

1) Achieving a high unloaded Q (70 ~ 200) for inductors on substrates with thicknesses in the range of 100 – 140 microns in the frequency range of 1 – 20 GHz. The novelty in the objective lies in solving the issue of reduced ground separation of the inductors , thereby attempting to overcome the parasitic capacitance issue which is the major bottleneck in achieving a high unloaded Q
2) Achieving the high unloaded Q within a reduced form factor and at the same time catering to the inductance values required for RF applications. Given the thickness of the thin substrate, the objective is also to achieve the high Q and inductance in the smallest volume density.

In a nutshell, the research objectives are as shown in Figure 1.18

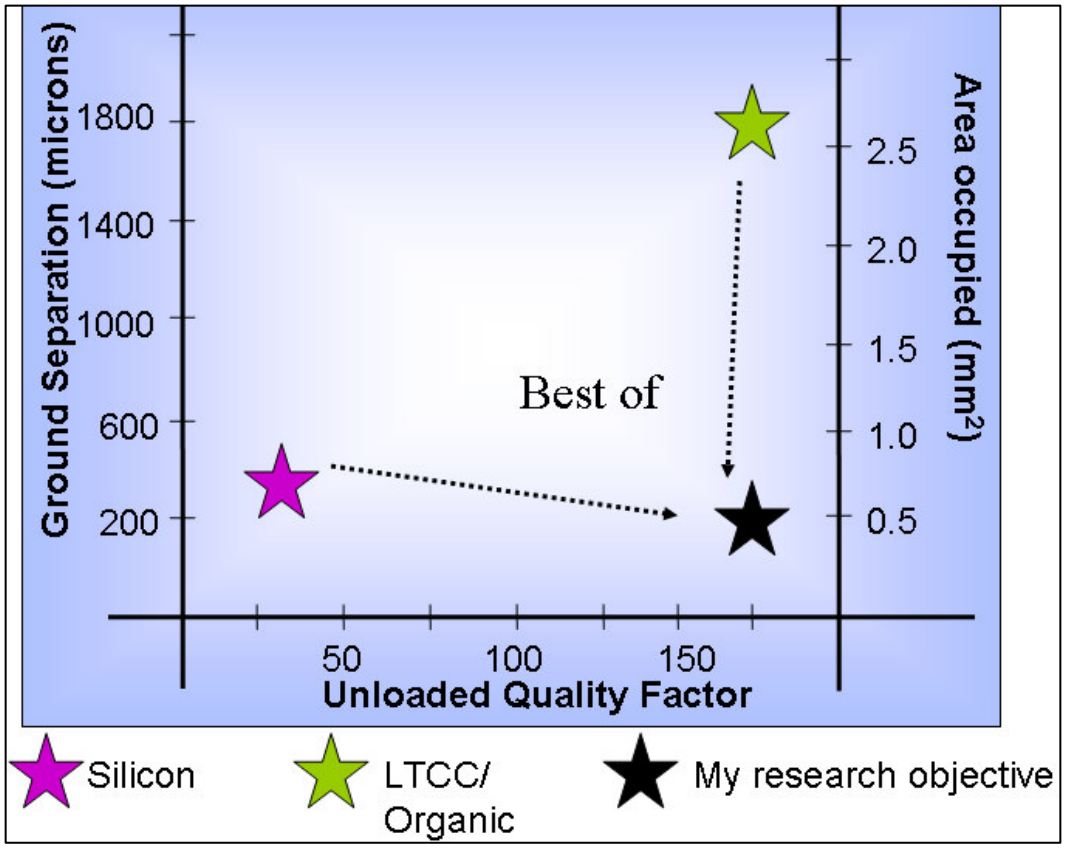


Figure 1.18 Objectives of Research

The current work aims at bringing together the best of Silicon and LTCC/Organic technology in the area of RF high Q inductor integration

CHAPTER 2

DESIGN, FABRICATION AND CHARACTERIZATION OF EMBEDDED INDUCTORS

High-Q passive components play a critical role in system performance in modern communication systems. They have a direct influence on the parameters such as phase noise. The Q of the inductors affects these parameters. The embedded passives can provide very high-Q passives components for the inductors which are critical in tank circuits in VCO and gate inductor in source-degenerated LNA, thus leading to high performance circuits. But they take up real estate on the surface of the substrate or board if they are surface-assembled with traditional approaches (they occupy up to 70 – 80 % of real estate). Therefore, the SOP concept with embedded thin film components can provide a compact, low-profile solution without degrading system performance.

In this chapter, low profile inductors have been designed and fabricated in two test vehicles followed by fabrication and high frequency measurements. Good correlation has been shown between the designed and measured results by making use of a suitable de – embedding technique. The main contributions of this chapter are

1) Demonstration of high Q inductors in two ultra thin test vehicles.
2) Model to measurement correlation

2.1 Test Vehicles

Embedded planar and 3D inductors are designed and built in two test vehicles - test vehicle 1 (TV1) and test vehicle 2 (TV2) shown in Figure 2.1. TV1 consists of a core and two metal layers. The core is fabricated with a new family of ultra thin dielectric with

low loss and low dielectric constant (tan δ = 0.0037, ε_r = 3.48). The thickness of the core is 130 microns. These parameters are very stable over a frequency range of 1 – 10 GHz. The metal layers are about 15 -20 microns in thickness. TV2 consists of a core, two buildup layers and four metal layers. The core is of the same material and thickness used in TV1. The buildup layers are also from the same family of ultra thin low loss dielectrics and have a thickness of about 20 - 25 microns per layer with electrical properties tan δ =0.0043 and ε_r = 2.51. The four metal layers are of the same thickness as used in TV1. Given the number of metal layers in TV1 and TV2, planar inductors are designed in TV1 while 3D and planar inductors are designed in TV2.

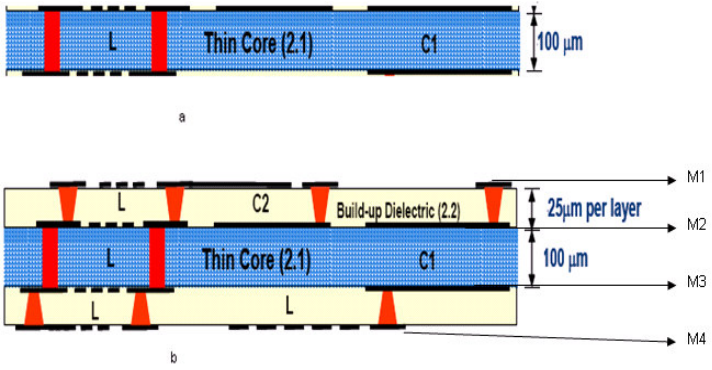


Figure 2.1 a.TV1 b.TV2

TV1 consists of mechanically- drilled through holes for backside connections while TV2 consists of laser drilled micro vias. The plated through holes in TV1 are about 100 – 200 microns in diameter and the microvias in TV2 are about 30 - 50 microns in diameter. More details about the test vehicles are given in the later sections.

2.2 Inductor Designs

Amongst the various factors affecting the quality factor for a given substrate and inductor topology, the most important contributor is the distance of ground plane separation. The greater the ground separation, the higher the achievable Q and hence this is the main challenge in designing and building inductors with the test vehicles described in the previous section. The effects of using a thin substrate can be further explained by Figure 2. 2.

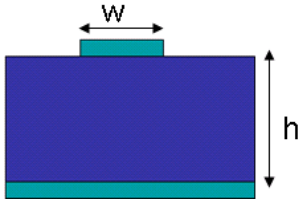


Figure 2.2 A microstrip structure

For the micro strip structure, shown in Figure 2.2, the capacitance due to the dielectric constant ε_r, is given by

$C_o > \varepsilon w/h$ (2.1)[10]

From this equation, it is clear that the capacitance is inversely proportional to the ground separation. This capacitance includes the parasitic capacitive coupling to ground. This parasitic capacitive coupling decreases the quality factor. The direct relationship between the quality factor and the ground separation at high frequencies is given by the equation

$Q < \mu/ \mu_c*(4h/\delta)$ (2.2) [10]

where δ is the skin depth, μ is the permeability of the material and μ_c is the permeability of free space. At RF frequencies, the skin depth is a major contributing factor to the losses associated with micro strip structures. From equation 4, it is clear that quality

factor is directly proportional to the value of ground separation and hence this is the main bottleneck in achieving high quality factors in ultra thin substrates. However, another inference that can be made from equation 4 is that the quality factor can be increased by the use of highly permeable magnetic materials ($\mu_c > 1$), but this is not possible in the present scenario where the permeability of the new class of organic substrates is $\mu_c = 1$. Keeping in mind the challenges explained in the previous section, several inductor design topologies have been exploited to achieve high unloaded quality factor values and desired inductance in the frequency range of 1 – 10GHz. Inductors have been designed in TV1 and TV2. Planar rectangular and circular spiral inductors are designed in test vehicle 1.The second metal layer was used as the ground for return currents. Cylindrical vias are used to connect to the ground layer. Figure 2.3 shows some of the planar inductor models. TV 2 (4 metal layer substrate) was used to design helical and 3D inductors. The helical inductors offer enormous area reduction for the same value of inductance achieved when compared to planar inductors. Also, the quality factor is increased as the distance at which the overlap of the successive half turns takes place is increased. In both the 2D and 3D designs, the advantages of the organic laminate process in achieving very thin lines have been exploited. To this effect, the line width and spacing used in these inductor designs are of the order of 50 – 100 microns.

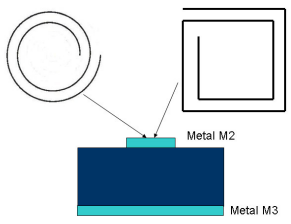


Figure 2.3 Some planar inductor designs

2.3 Topology Modification - Patterned Ground

In order to overcome the problem of reduced ground separation and achieve high unloaded quality factor of inductors, patterned ground has been used. The effect of using a patterned ground plane can be explained from the effects of increasing the line width of the turns of the spiral inductor. Increasing the line width increases the quality factor by reducing the series resistance. This however increases the parasitic capacitive coupling to ground. The effect of the substrate capacitance on quality factor is as shown in Figure 2. 4. [26]

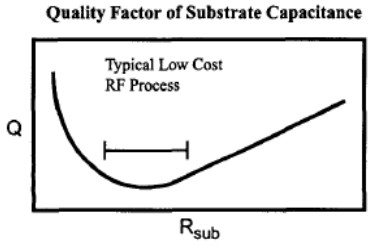


Figure 2.4 Relationship between Q and substrate capacitance

So, the aim is to reduce the quality factor of this parasitic capacitance to ground while taking care to not increase its magnitude. This is accomplished by the use of patterned ground planes. As will be explained in the successive sections, patterned ground planes provide an increase of about 40% in the quality factor of the inductor maintaining the same self resonant frequency and the frequency at which highest Q is achieved.

2.4 Electrical Modeling of Inductors on TV1

The inductors were modeled using an electromagnetic tool, SONNET [27] which calculates the fields based on the method of moments technique. The model of the inductor designed in SONNET is shown in Figure 2.5

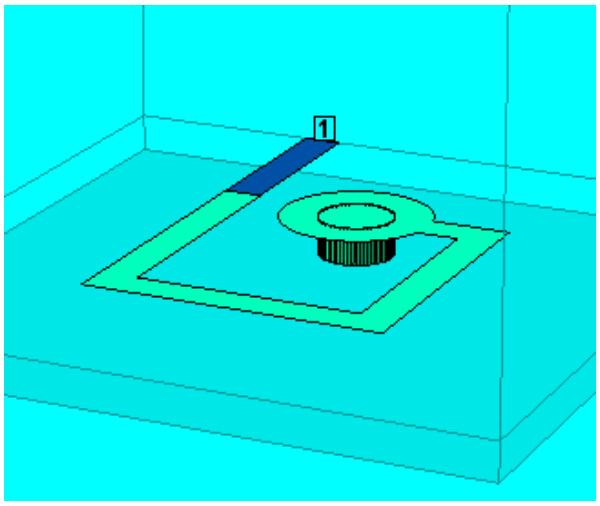


Figure 2.5 Model of inductor on TV1 in SONNET

Fig. 2.5 shows a single turn rectangular spiral in metal layer M2. The spiral is connected to the ground layer (metal M3) using a cylindrical hollow via. The top view of this design is shown in Figure 2.6.

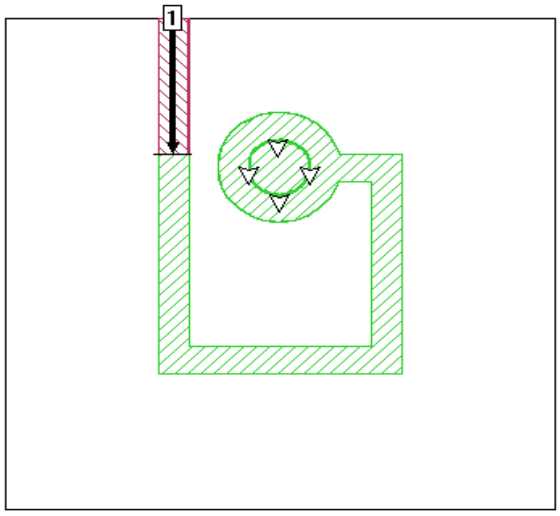


Figure 2.6 Top view of model on TV1 in SONNET

A total of 16 inductors were designed with different metal widths, spacing and number of turns to achieve various values of inductance densities and quality factors for a given

frequency range. The widths and spacing of the inductors used in these 16 designs ranged from 50 microns to 200 microns. The area occupied by the inductors was also optimized to obtain the highest inductance in the smallest area possible. In this context, the area occupied by the inductors ranged from 0.7 mm^2 to 1.4 mm^2. A summary of the inductor designs geometries is given in Table 2.1 and the associated inductance and quality factor is given in Table 2.2 .

Table 2.1

Table 2.1 Inductor design geometries on TV1

Design	Number of turns	Width (microns)	Spacing (microns)	Area(mm2)
D12	1	100	100	0.764
D13	1	200	125	1.125
D14	1	300	125	1.029
D3	1	120	160	1.03
D15	1	200	150	1.3125
D16	0.5	200		0.742
D17	1	50	50	0.785
D18	1	50	50	0.45

A comparison of the inductances and quality factors of these inductors is shown in Figures 2.7 and 2.8

Table 2.2 Inductance, Q and SRF

Design	SRF (GHz)	Highest Q	Frequency of highest Q	L (nH)
D12	22	58	9	1.06
D13	17	73	7	0.83
D14	20	82	9	0.52
D3	20	64	8.5	1.2
D15	18	75	8	0.89
D16	28	94	12	0.57
D17	19	43	8	1.58
D18	26	50	12	1.06

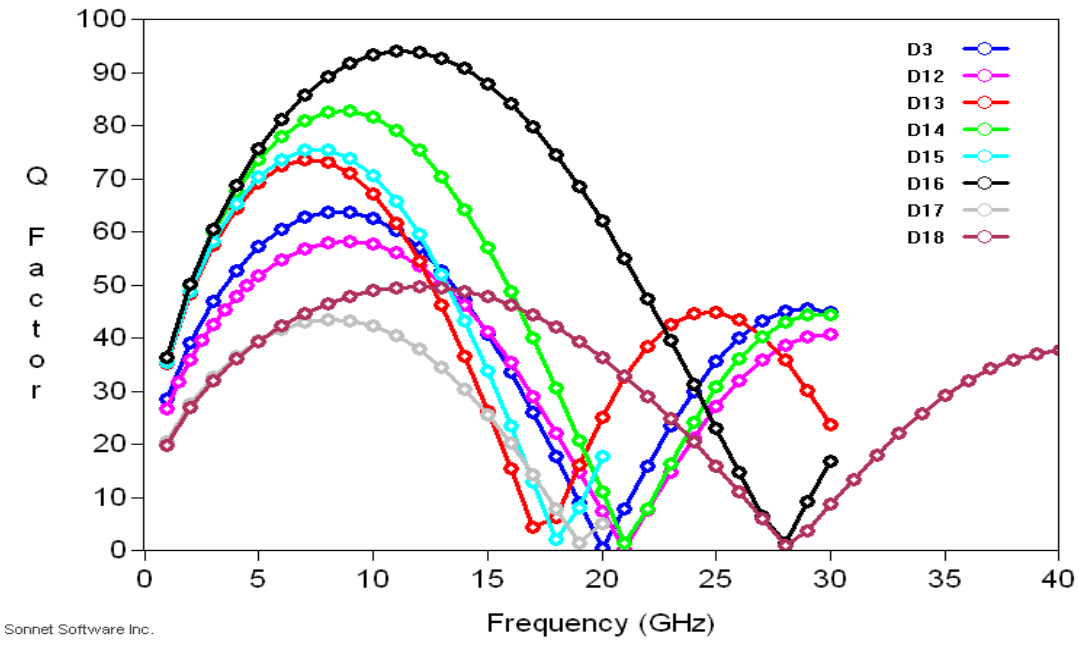


Figure 2.7 Q factors of inductors with whole ground in TV1

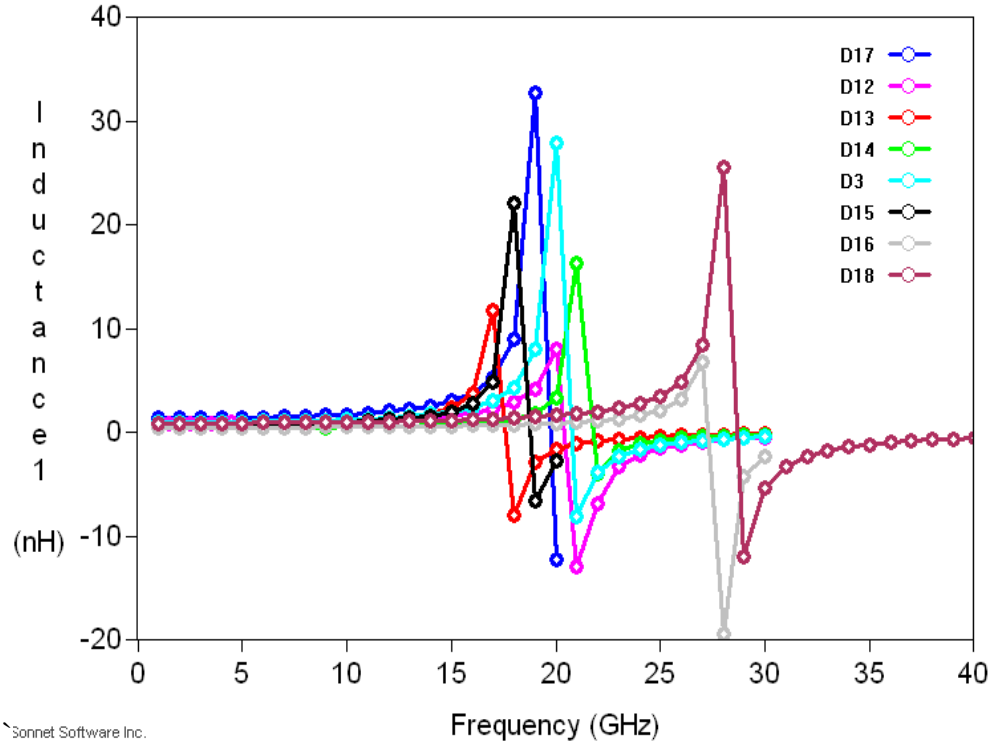


Figure 2.8 Inductance of inductors with whole ground in TV1

As can be seen from the data Tables and associated graphs, a maximum quality factor of 94 was achieved for design D16 with SRF of about 28 GHz. This is a half turn spiral design with a ground separation of 100 microns. However, the inductance achieved for this inductor was the lowest at around 0.57nH in an area of 0.742 mm^2. The inductors designed on TV1 provide good scalability in terms of L, Q and SRF and hence can be used at different frequencies of interest.

As explained in the previous sections, the minimal ground separation of 100 microns serves as a major bottleneck in achieving unloaded Q's of greater than 100 within the specified design rules. Hence a set of inductors was designed with patterned ground. These inductors were also designed in SONNET and the top and 3D view is shown in

Figures 2.9 and 2.10. The patterned ground is modeled as a rectangular piece of metal on layer M3. In the SONNET model, the bottom metal is declared as free space to facilitate accurate simulation of this design. Table 2.3 and 2.4 show the details of the geometry and the electrical parameters. As can be seen from the Table 2.4, there is an

Table 2.3 Geometry details for patterned ground inductors

Design	Number of turns	Width (microns)	Spacing (microns)	Area(mm2)
D12_1	1	100	100	0.764
D13_1	1	200	125	1.125
D14_1	1	300	125	1.029
D3_1	1	120	160	1.03
D15_1	1	200	150	1.3125
D16_1	0.5	200		0.742
D17_1	1	50	50	0.785
D18_1	1	50	50	0.45

Table 2.4 Inductor designs with patterned ground

Design	SRF (GHz)	Highest Q	Frequency of highest Q	L (nH)
D12_1	20	93	9	1.96
D13_1	20	130	10	0.83
D14_1	24	134	12	0.94
D3_1	23	100	10	1.95
D15_1	21	135	10	1.54
D16_1	24	205	11	1.52
D17_1	19	65	8	2.42
D18_1	26	71	12	1.7

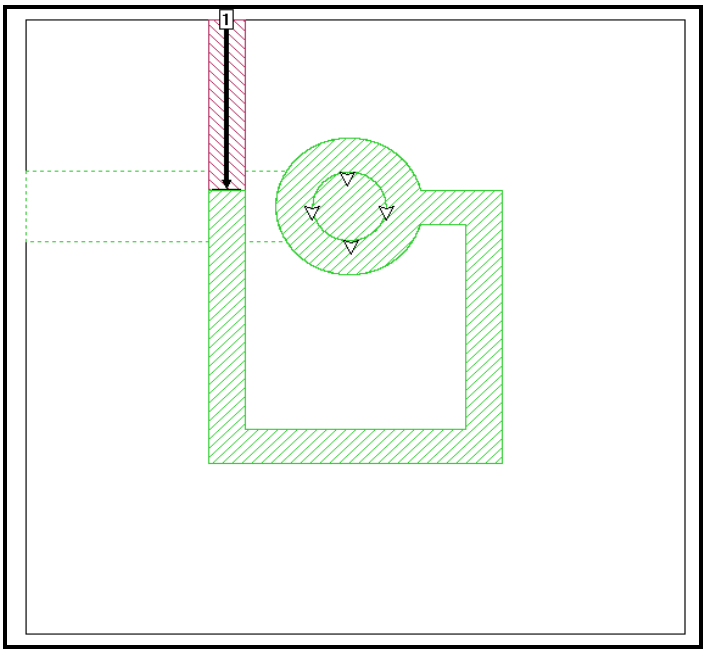


Figure 2.9 Top View of patterned ground inductor on TV1 in SONNET

increase of about 40% in the Q of the inductors for about the same frequency of interest. This comparison is shown more clearly in Figure 2.11 which compares the Q of design D12 for the whole ground and patterned ground cases. The inductance is found to increase (Figure 2.12) in the case of the patterned ground inductors. This is attributed to the reduction of the parasitic capacitance and hence an increase in the value of inductance for the same area occupied by the inductor.

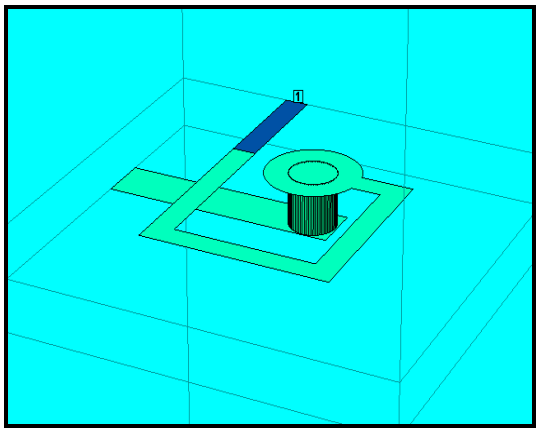


Figure 2.10 3D view of patterned ground inductor on TV1 in SONNET

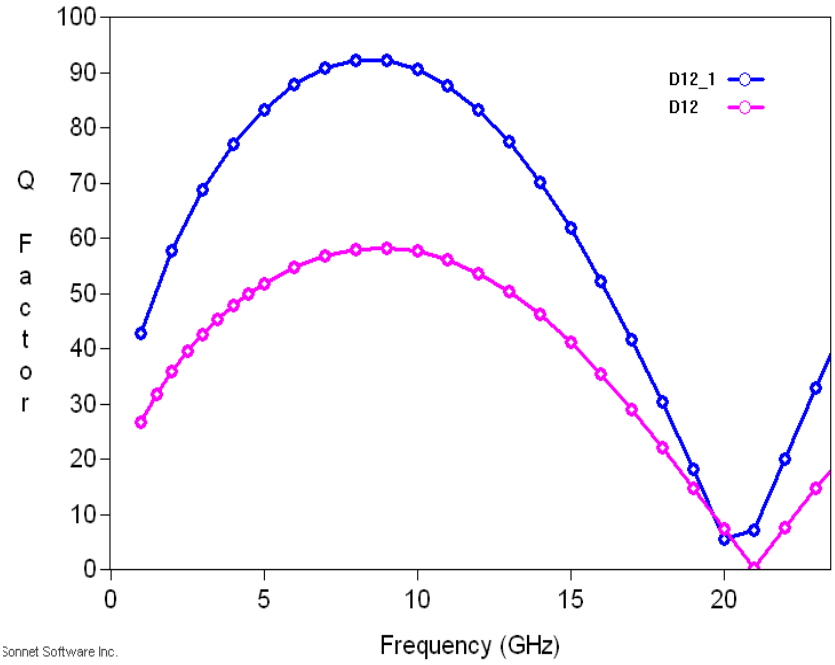


Figure 2.11 Comparison of D12 for whole and pattered ground - Q

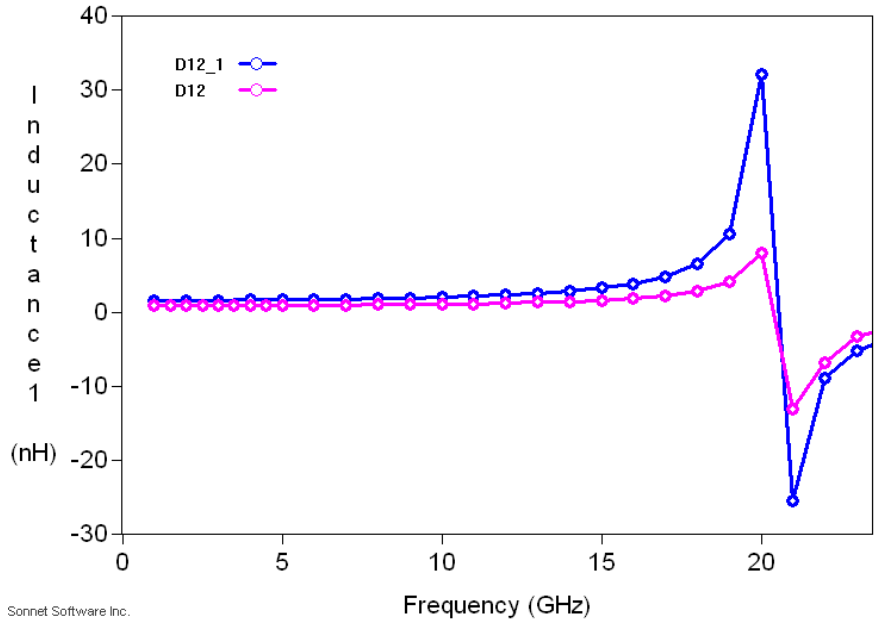


Figure 2.12 Comparison of D12 for whole and pattered ground - L

2.5 Measurements

The measurements were performed using the Agilent Vector Network Analyzer with probing stations. A GSG 250 micron air probe was used to probe the structures. The measurements were done for a frequency range of 1 – 18 GHz. In order to emulate the suitable conditions for testing of patterned ground inductors, the test vehicle was placed on a bare FR4 board which was in turn placed in the probing station. This helped to prevent the shorting of the whole and patterned grounds of all the inductor structures. Figs. 13 and 14 show the measurement vs. model results for design D13. The values of Q presented in this Table have been averaged from the measurements made. As can be seen from Table 2.5 and Figures. 2.13 and 2.14, there is a good correlation between the model and measured values. The highest measured Q for D3 is 80 at a frequency of 9GHz while the modeled value is 64 at a frequency of 8.5GHz. This shows that the measured Q's are

higher than the modeled values. This trend is also seen for designs D3, D17 and D18. The reason for this difference in Q is that the EM solver SONNET always over predicts the losses associated with the inductor and hence under predicts the value of Q. Also the measured inductance is higher than the modeled value for all the designs presented here. This is because the measured inductance includes the inductance of the probe pads and the connector joining the end of the inductor to the probe pad. The SRF for designs D14, D16 and D18 could not be measured due to limitations in the calibration range of the GSG probe available.

However, as can be seen from Figures. 2.13, 2.14 and Table 2.5, the measured inductance does not correlate with the modeled inductance at higher frequencies. Also, there is a difference in the measured SRF. In particular, there is a difference of about 1-4 GHz in the measured SRF and about 0.6nH in the measured inductance This could be due to the inductance provided by the probe pads and the connecting microstrip line between the inductor and the probe pad, as mentioned earlier This effect can be moderated by a suitable de – embedding technique as explained further.

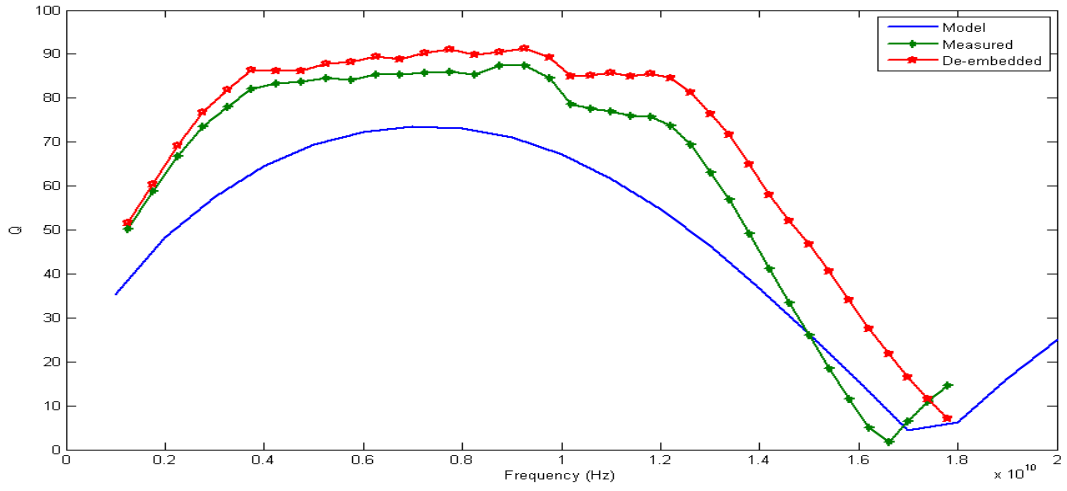


Figure 2.13 Measured vs. modeled Q for D13

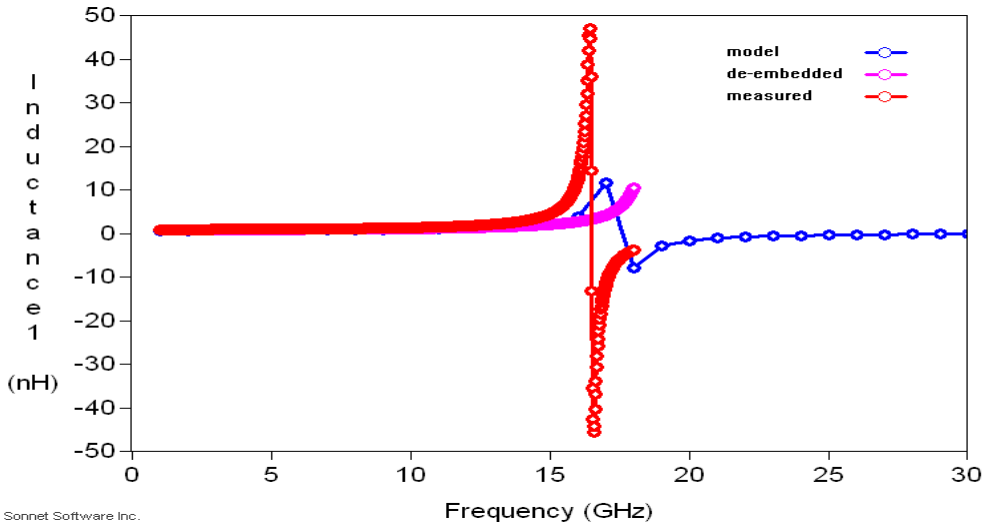


Figure 2.14 Measured vs. modeled inductance for D13

Figures 2.15 and 2.16 show the comparison between measured and modeled results for patterned ground inductor design D17_1. There is a shift in the resonance frequency and a highest Q of about 66 is obtained at 5.25GHz.

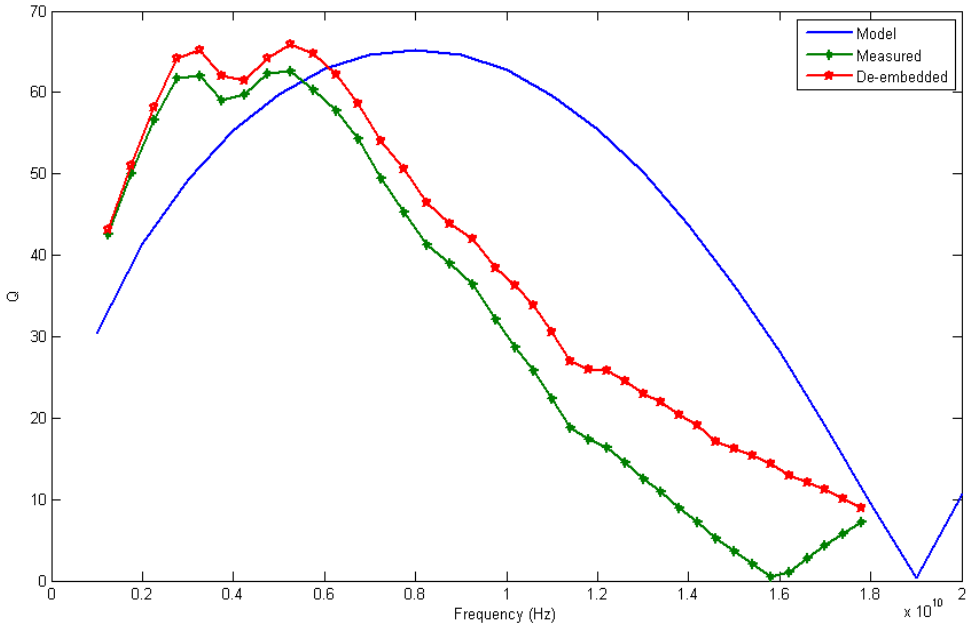


Figure 2.15 Measures vs. modeled Q for D17_1

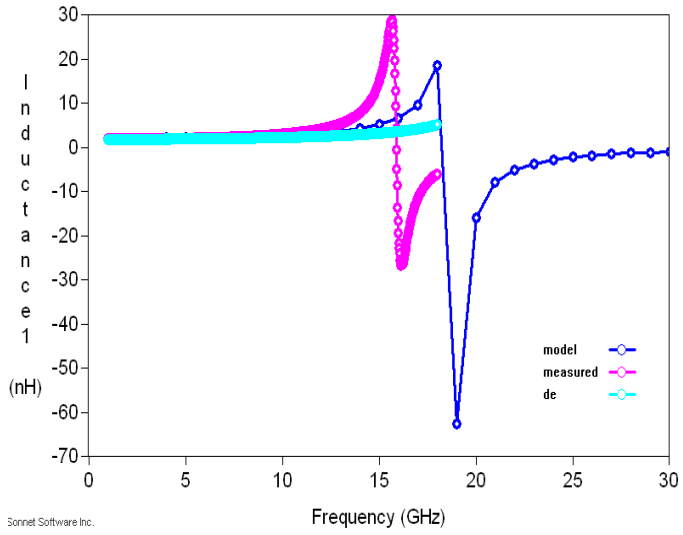


Figure 2.16 Measured vs. modeled inductance for D17_1

Table 2.5 Measured results

Design	SRF (GHz)	Highest Q	Frequency of highest Q	L (nH)
D13	16.5	88	9	1.26
D14	***	92	9.5	0.72
D3	16	80	9	1.86
D15	15	70	9.25	1.53
D16	***	110	13.4	0.75
D17	17.5	70	8.75	2.05
D18	***	82	12.7	1.57

Table 2.6 De – embedded results

Design	SRF (GHz)	Highest Q	Frequency of highest Q	L (nH)
D13	17.5	91	9	1.08
D14	***	95	9.5	0.63
D3	18	87	8.5	1.51
D15	17	75	9.75	1.35
D16	***	112	13	0.93
D17		75	9.75	1.8
D18	***	93.75	13.5	1.21

2.6 De - Embedding

A suitable de- embedding technique is shown [28].The technique used in this paper is a slight modification from [28] in which the parasitics are considered to be parallel in the probepads and series in the connector. The steps followed in this de –embedding process is shown in Figure 2.17 as a flow chart. Using these steps to de-embed the test structures, the inductance and Q of design D13 after de-embedding is shown in the Figures. 2.13 and 2.14 and in Table 2.6 for all the other designs. As can be seen from the results presented, the measured SRF agrees well with the modeled SRF. The difference in the measured SRF and modeled SRF is about 1GHz after de-embedding.

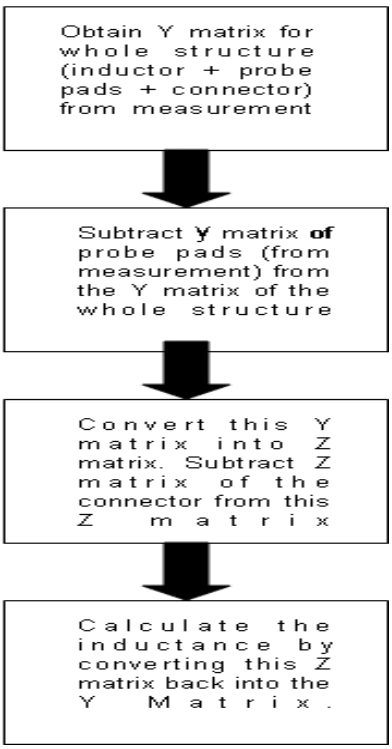


Figure 2.17 Flowchart for de - embedding

2.7 Layout and Fabrication

The layout of test vehicle 1 consisted of a total of 64 inductors, comprising of whole and patterned ground structures. The structures were duplicated to ensure better yield from the fabrication process and enable in making consistent measurements. The probe pads were designed as coplanar GSG pads with a pitch of 250 microns. The dimensions for the vias and via pads are 200 microns and 400 microns respectively. The layout was made in CAM350 and Figure 2.18 shows the layout of a single inductor and the entire layout of the test vehcile as designed in CAM 350. The GSG probe pads were added as individual structures to enable in obtaining data for the de – embedding process after measurements.

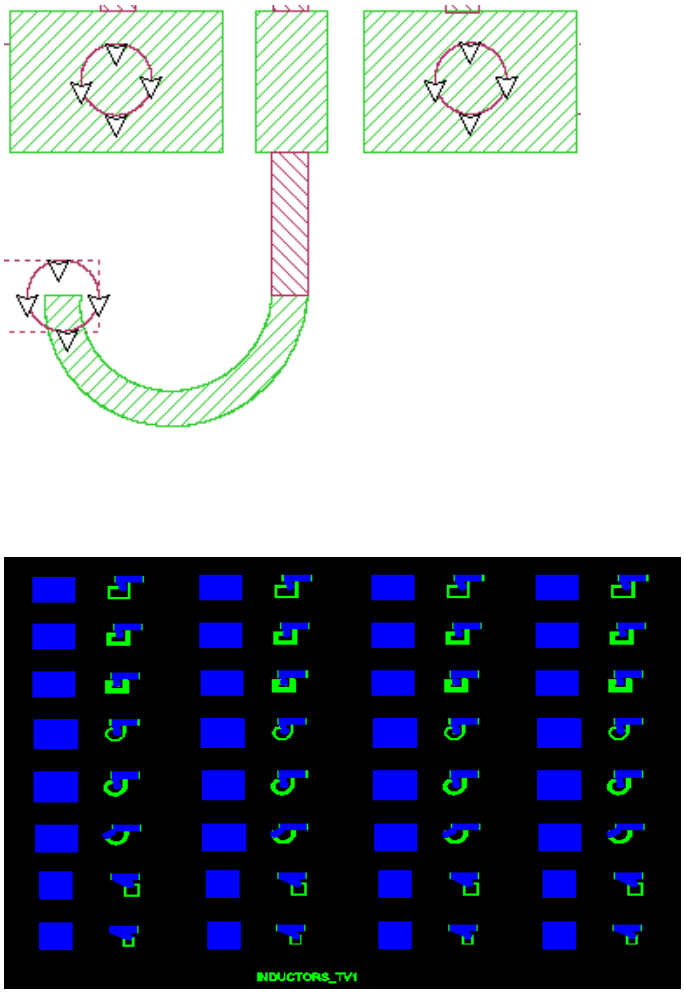


Figure 2.18 Layout of inductor test vehicle

The inductors were fabricated in the PRC cleanroom. The steps followed in the fabrication process are as follows

1. Mechanical drilling
2. Electro less and Electrolytic copper plating
3. Photo resist Lithography
4. Etching
5. Photo resist Stripping

Some pictures of the fabricated inductor are shown in Figure 2.19 .The inductor test vehicle is shown in Figure 2.20

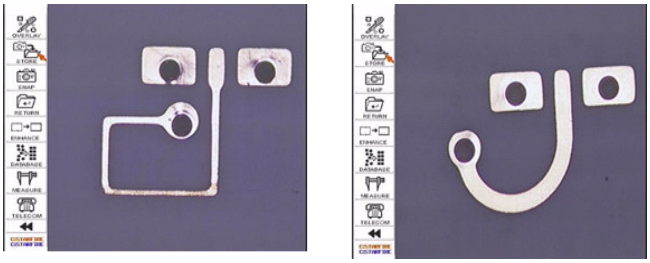


Figure 2.19 Fabricated Inductors on TV1

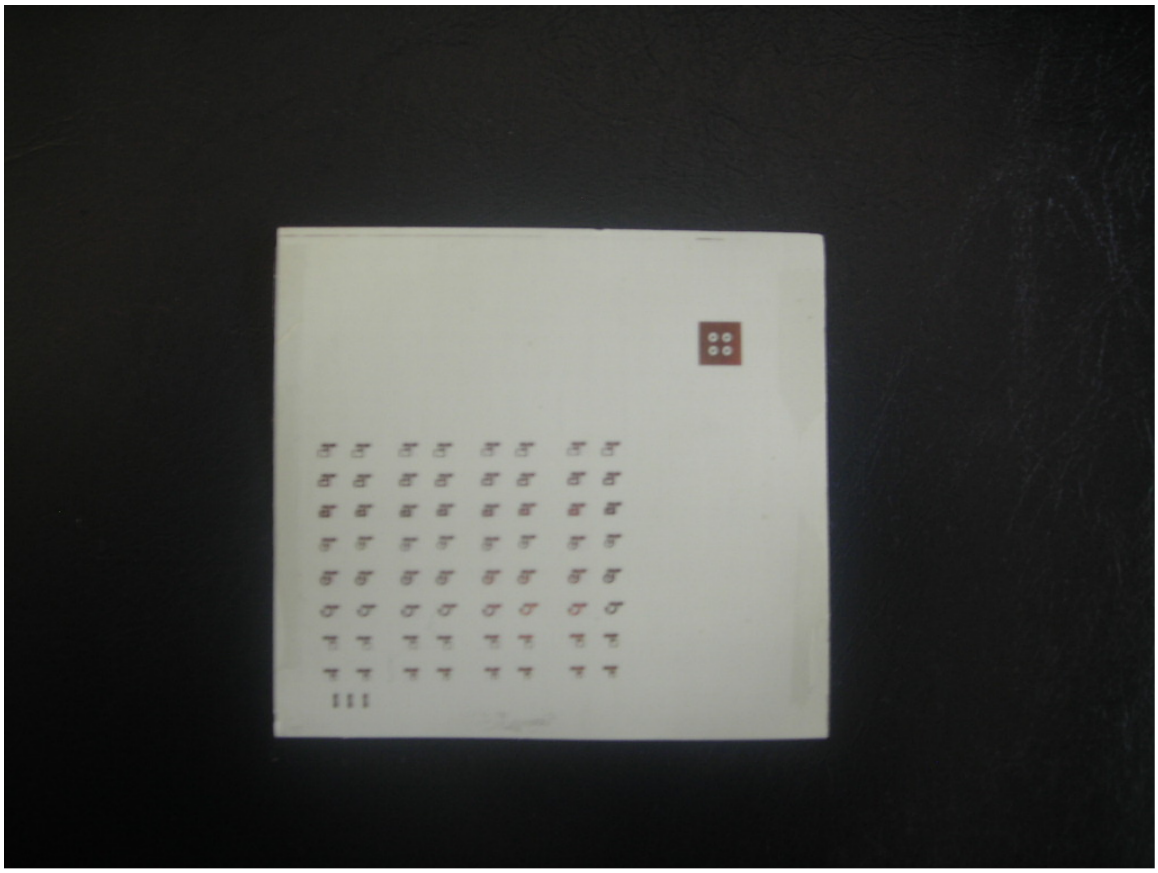


Figure 2.20 Fabricated Inductor test vehicle

2.8 Electrical Modeling of Inductors on TV2

3D and planar inductors were designed in TV2. The planar inductors were designed on M1 with M4 as the ground layer. The 3D inductors were designed using layers M1, M2 and M3 with M4 as ground. The top view of the planar and 3D inductors is shown in Figure 2.21. The planar inductors designed on TV2 were similar to those designed on TV1 except for the distance of ground separation.

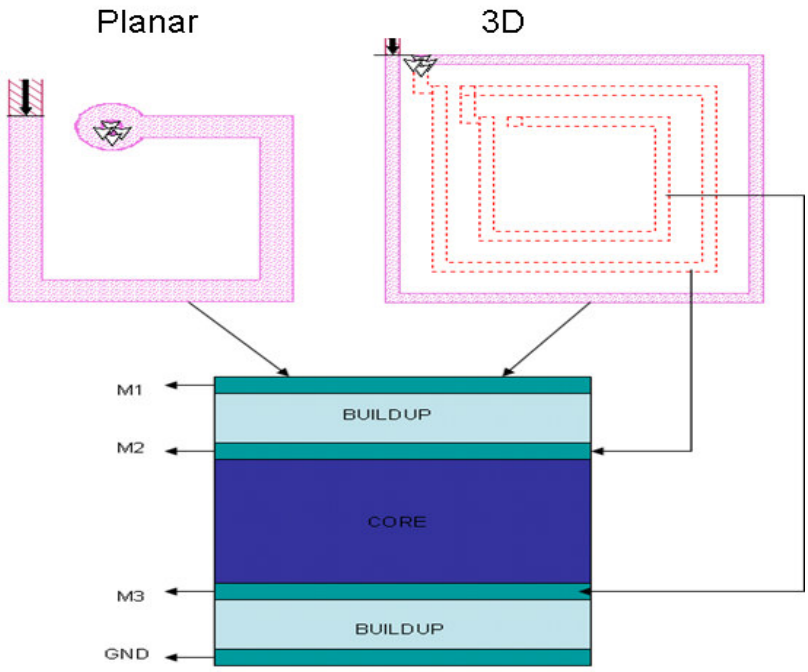


Figure 2.21 Inductors on TV2

The ground separation for TV2 is about 140 microns. This enables us to get higher Q's for planar inductors on TV2 when compared to similar designs on TV1.

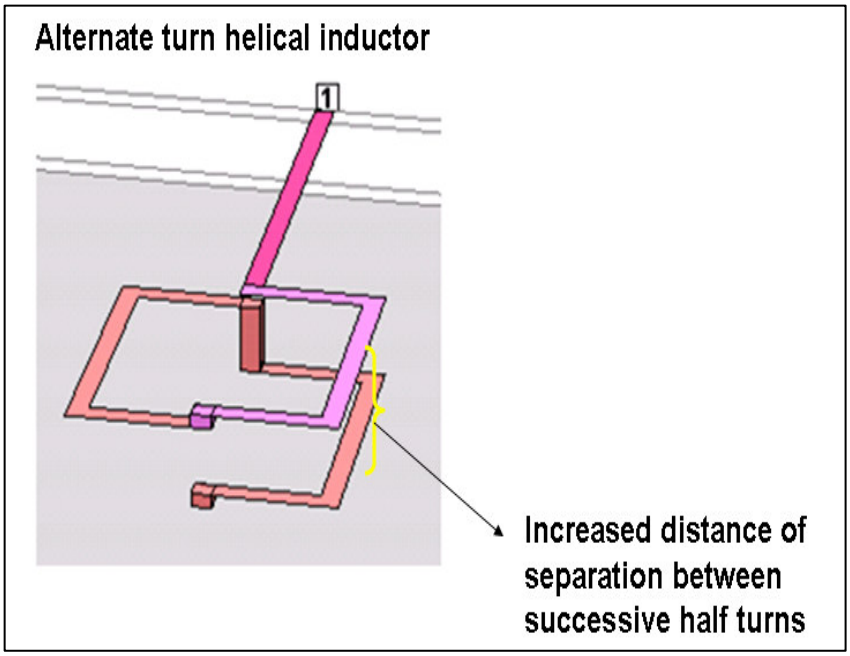


Figure 2.22 a Alternate turn Helical Inductor

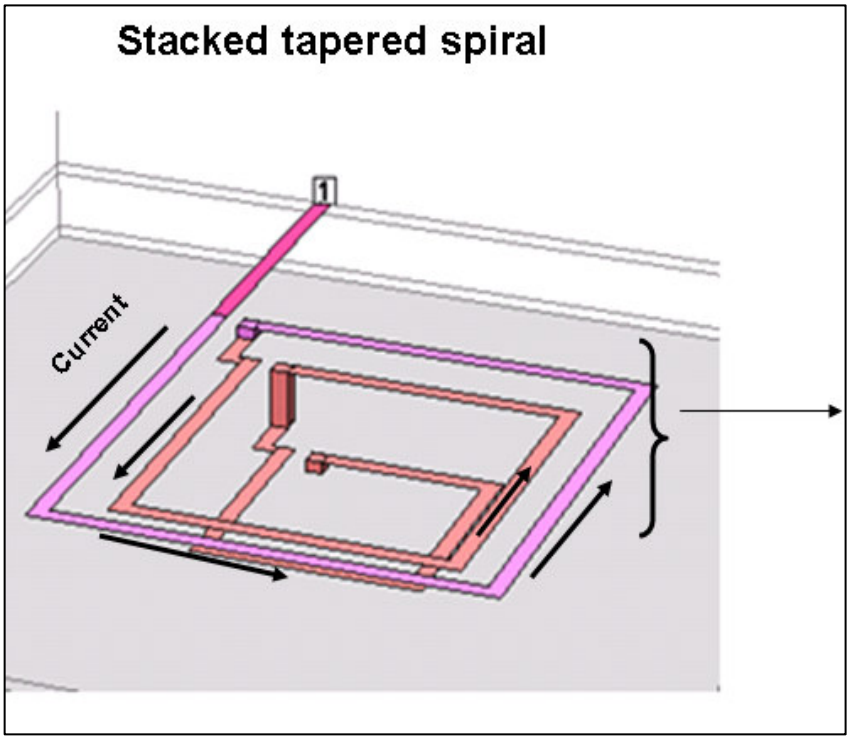


Figure 2.22 b Tapered Spiral Inductor

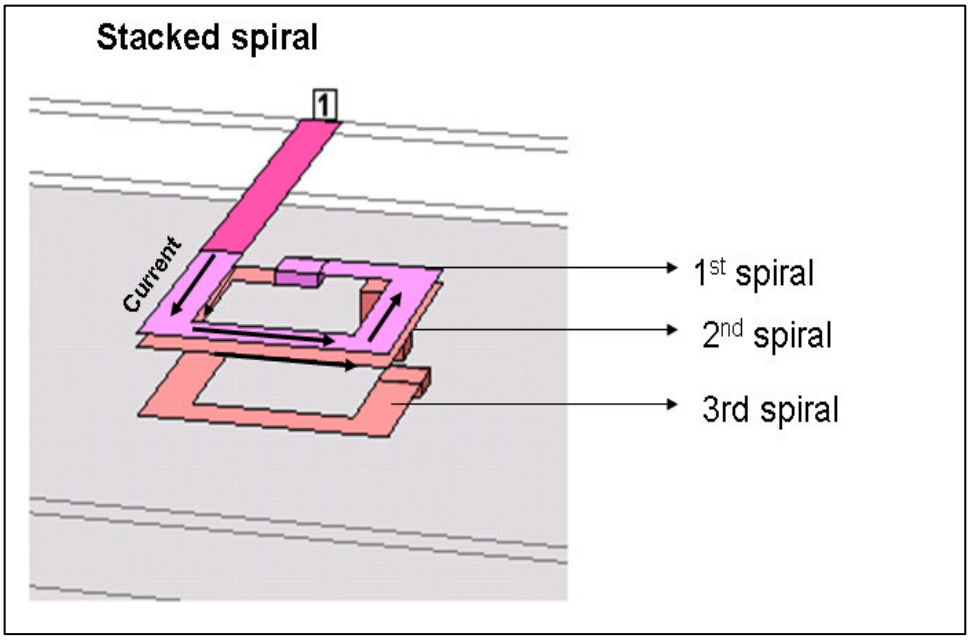


Figure 2.22 c Stacked Spiral Inductor

The 3 D inductors that were designed in TV2 comprised of stacked spiral, helical and tapered spiral. These designs are shown as SONNET models in Figure 2.22. The stacked spiral design consists of rectangular or circular spirals on the three metal layers connected by cylindrical vias. The designs an be altered to enable the flow of current in the same direction or opposite directions in the three spirals so as to change the polarity of the mutual inductive coupling which in turn relates to the total inductance achieved. This change of current directions can be enabled by positioning the vias in the appropriate places. The tapered spiral designs are similar to the stacked spiral designs except that they take advantage of the absence of the parasitic capacitive coupling between the successive layers and hence enable higher Q values to be achieved. The third type of 3D design is the helical design which consists of half turn spiral on each of the three metal

layers such that the successive half turns do not overlap. This increases the distance between two half turns and hence aids in reducing the parasitic capacitive coupling. The details of the geometry of the design is shown in Table 2.7. Modeled results for these three types of 3D inductors and planar shown in Table 2.8

Table 2.7 Geometry details of 3D inductors

Design	Width (microns)	Spacing (microns)	Area(mm2)
3D_1(AHT123)	30	30	0.64
3D_2(AHT123)	30	30	0.36
3D_3(AHT123)	30	30	0.16
3D_4(AHT123)	70	70	0.36
3D_5(AHT123)	70	70	0.16
3D_6(AHT13)	70	70	0.16
3D_7(AHT13)	70	70	0.36
3D_8(FT13_Isame)	70	70	0.36
3D_9(FT13_Isame)	70	70	0.16
3D_10(FT13_Isame)	70	70	0.64
3D_15(planar spiral)	100	100	0.36
3D_16(planar)	70	70	0.36

Table 2.8 Modeled results for 3D inductors

Design	SRF (GHz)	Highest Q	Frequency of highest Q	L (nH)
3D_1(AHT123)	13	21	5	3.1
3D_2(AHT123)	18	25	8	2.3
3D_3(AHT123)	29	29	12	1.38
3D_4(AHT123)	23	37	9	1.28
3D_5(AHT123)	37	42	17	0.62
3D_6(AHT13)	50	50	24	0.4
3D_7(AHT13)	31	40	14	0.7
3D_8(FT13_Isame)	17	30	7	1.74
3D_9(FT13_Isame)	31	37	12	0.91
3D_10(FT13_Isame)	16	33	6	1.98
3D_15(planar spiral)	31	70	13	0.85
3D_16(planar)	32	61	14	1.08

2.9 Measurement- based inductor model

The designed inductors were measured using Agilent VNA with the SOLT calibration, combined with additional on-board structures to implement the de-embedding procedure. Since the thin substrate can be assumed as lossless, the dielectric loss can be ignored and an equivalent model can be simplified as Figure 2.23. A parallel capacitance (Cp) can be

determined from the SRF as in (2.3), and a series resistance (Rs) can be calculated from the Q as in (2.4). In (2-3), L is inductance, and Cp is the parallel capacitance. With the initial values of L and Cp, the values of L, Cp, and R for the designed inductors in TV1 were optimized in Agilent ADS, and model-to-hardware correlations are shown from Figures 2.24 and 2.25

$$\omega^2 = \frac{1}{LC_p} \tag{2.3}$$

Q = imag (Zin) / real (Zin) (2.4)

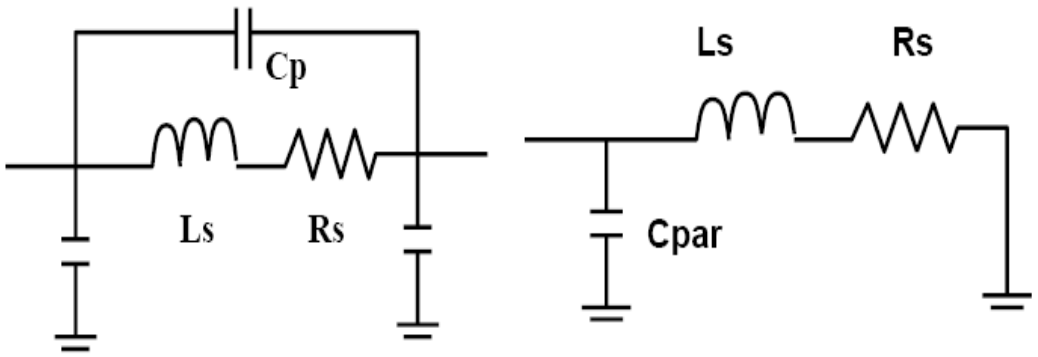


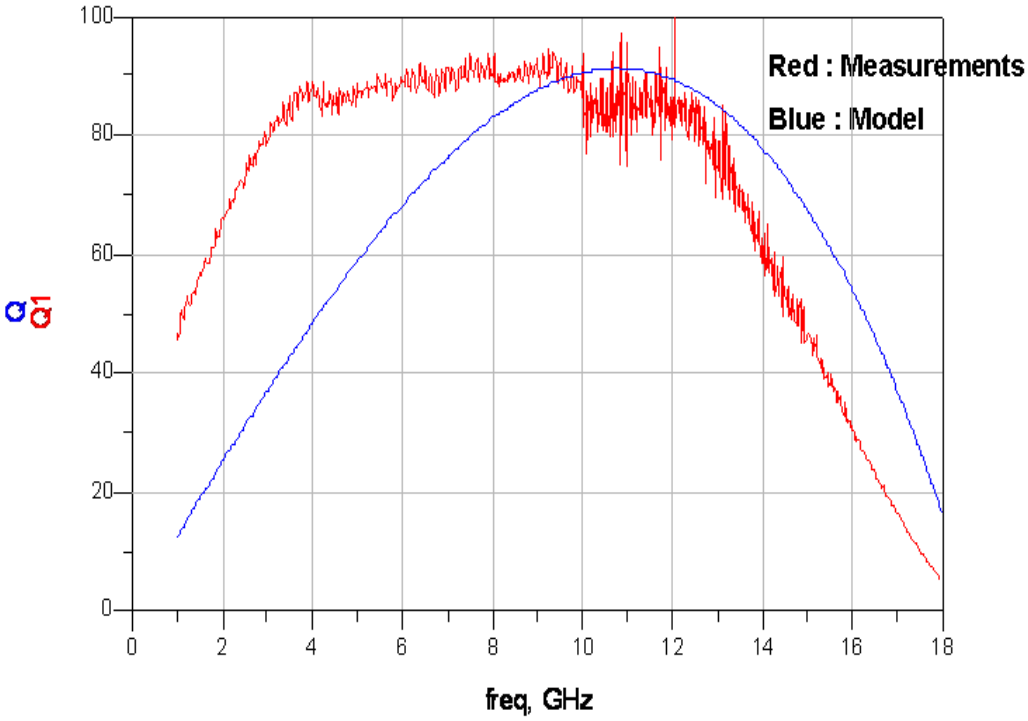
Figure 2.23 a . 2 port inductor model b. 1 port inductor model

The extracted parameters are shown in Table 2.9.

Table 2.9 Extracted parameters of the model

	Rs (ohms)	Ls (nH)	Cp (pF)
D13	0.6	1.2	0.06
D14	0.12	0.22	0.3
D3	0.82	1.54	0.04
D15	0.74	1.34	0.06

The model to measurements correlations for some designs are shown in Figures 2.24 and 2.25



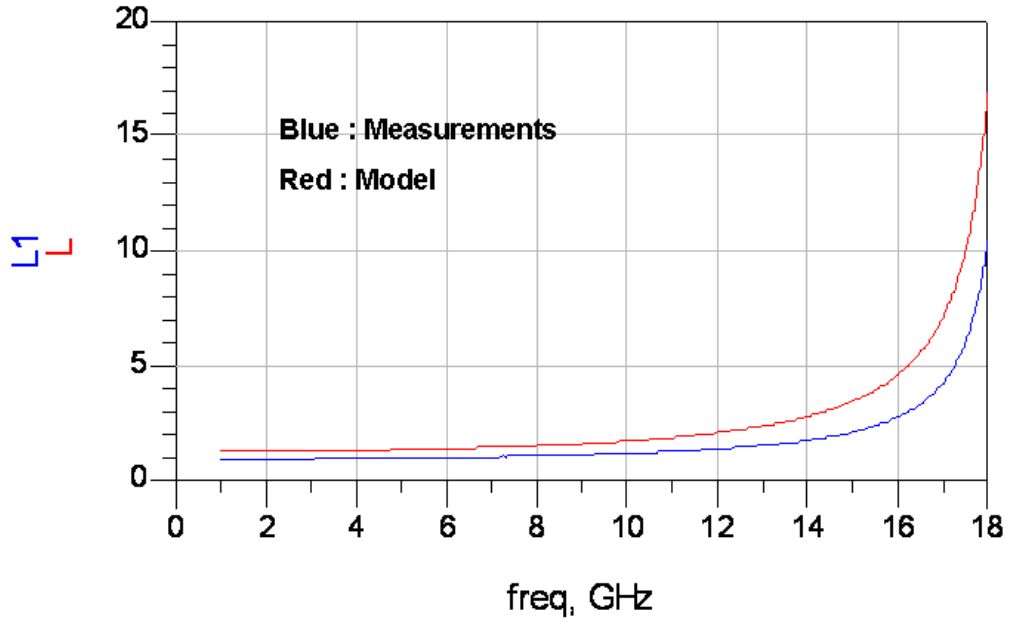


Figure 2.24 a and b model to hardware correlation for D13

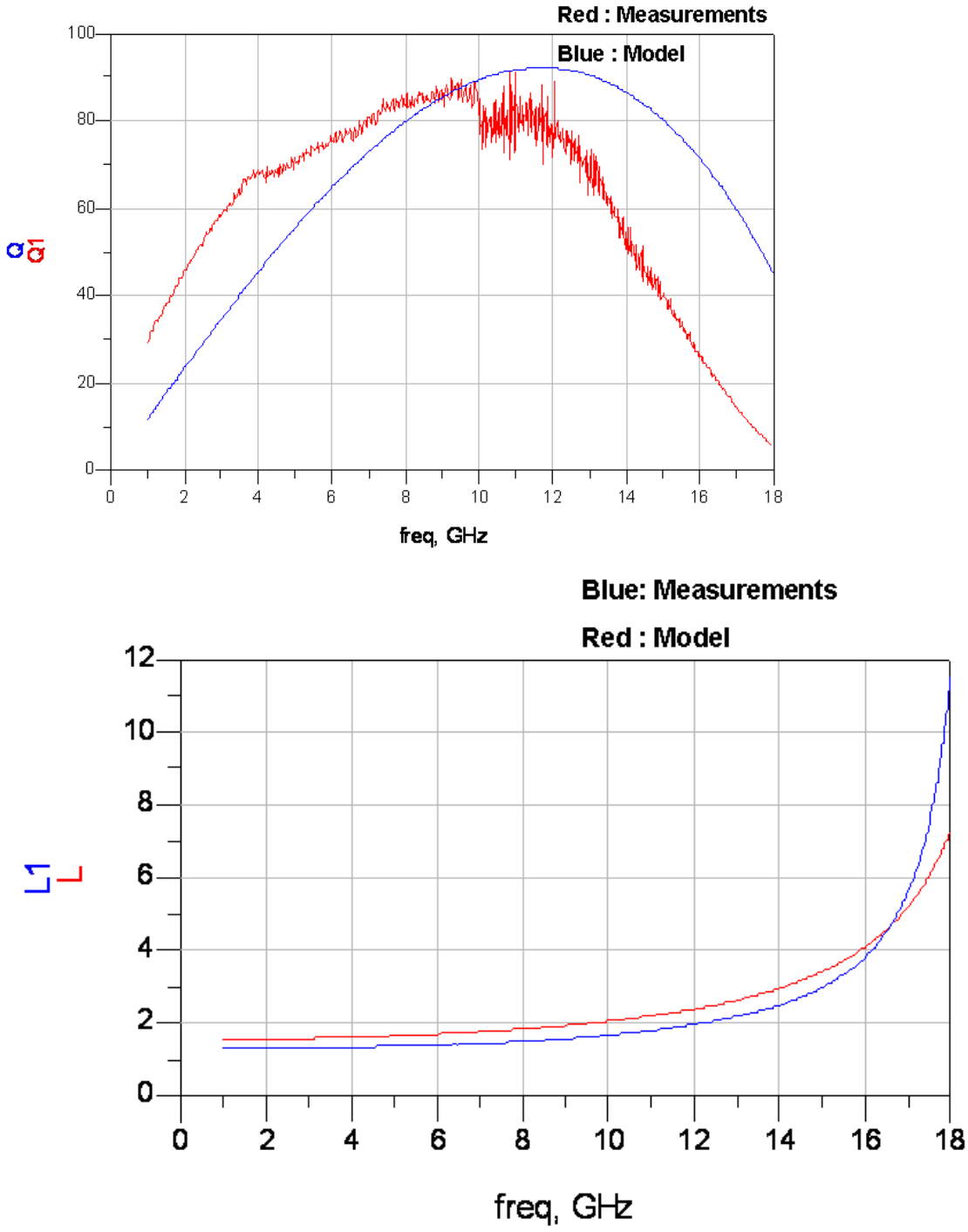


Figure 2.25 a and b Model to hardware correlation for D3

2.10 Conclusion

A detailed explanation of the design, modeling, fabrication and measurements for inductors in ultra thin substrates is given in this chapter. Whole ground and patterned ground inductors have been designed in substrates of thicknesses of the order of 100 – 140 microns. 3D inductor designs have been exploited for higher inductance density. An accurate model for single- port inductors has been provided and the parasitics have been extracted efficiently. The measured Q of the inductors is in the range of 70 - 150 with lateral inductance densities in the range of 1 – 5nH /mm2. The self resonant frequencies of these inductors are in the range of 10 -30 GHz. In the perspective of volume density of the inductors, as explained chapter one, the current work details the design of these high Q inductors in a volume which is at least an order lower than the published literature. This is the unique contribution of the current work.

The next chapter explains the use of these inductors in designing filters for a proof- of-concept demonstration

CHAPTER 3

PROOF OF CONCEPT FILTER DESIGN

The previous chapter showed the feasibility of obtaining high Q inductors (Q ~ 70 – 150) for RF applications on substrates of thickness 100 – 140 microns. This chapter discusses the use of these inductors in the implementation of filters for RF applications. Proof of concept demonstration of filters on the thin substrates is presented in this chapter.
The front end section of receivers such as homodyne and heterodyne is as shown in Figure 3.1

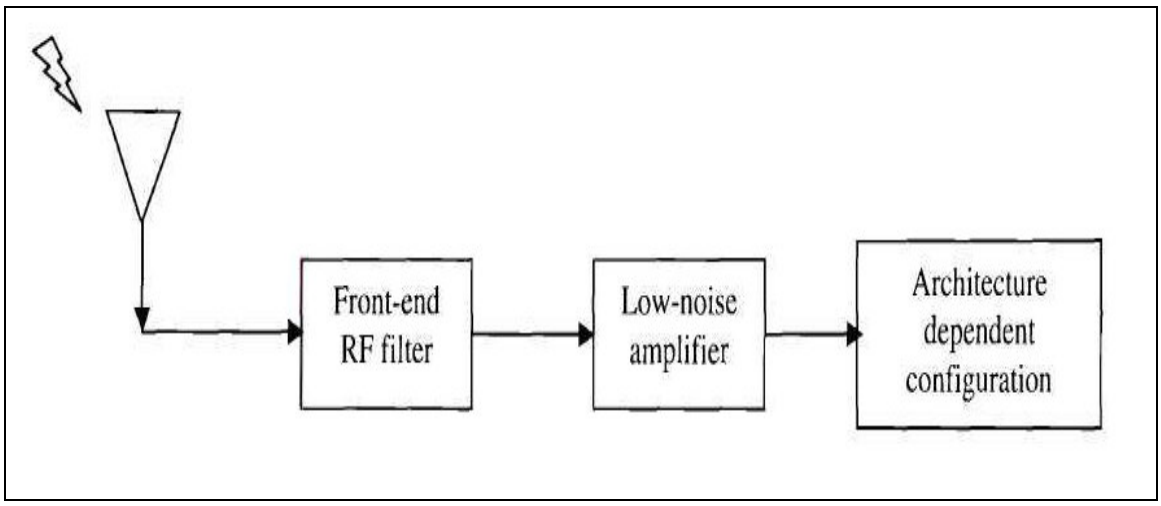


Figure 3.1 Front end section of a receiver

Rejection of image signals and removal of out band energy are the major functions of the RF front end filters. For most of the current RF standards, there is a rise in the center frequency towards the higher GHz range. This is becoming a major problem in designing filters for these applications. The demand on the unloaded Q of the components that

make up the filter - such as inductors ,capacitors and resonators is increasing as the loaded Q requirements is higher to suit the high center frequency applications. Some of the popular filters that are used in today's communication systems such as cellular phones are of the coaxial or monoblock types. They are preferred due to their superior performance and low loss that is achieved due to the transmission line sections. However, these filters suffer from disadvantages such as difficulty in the manufacturing process and usage of high dielectric constant ceramic materials which result in a reduction of the effective wavelength in the medium. There has been extensive work done in the area of filters on ceramic substrates using LTCC technology [29 - 31]. These filters make use of a large number of layers to implement the filters and hence result in the usage of a thicker substrate as already mentioned in chapter 2. The multi layer ceramic filters come with the disadvantage of higher costs due to the non – traditional processes used in making the multilayer ceramic filters.

The successive sections demonstrate filters designed on 2 and 4 metal layer substrates, utilizing a low cost organic substrate compatible process.

3.1 Band pass filters

Most of the filters implemented in ceramic substrates make use of large length of transmission filters. Since the current organic substrate used in this research has a very low loss and dielectric constant, it makes a better candidate for applications such as high sped transmission and high SRF embedded inductors. The topology of band pass filters used in this dissertation is shown in Figure 3.2.

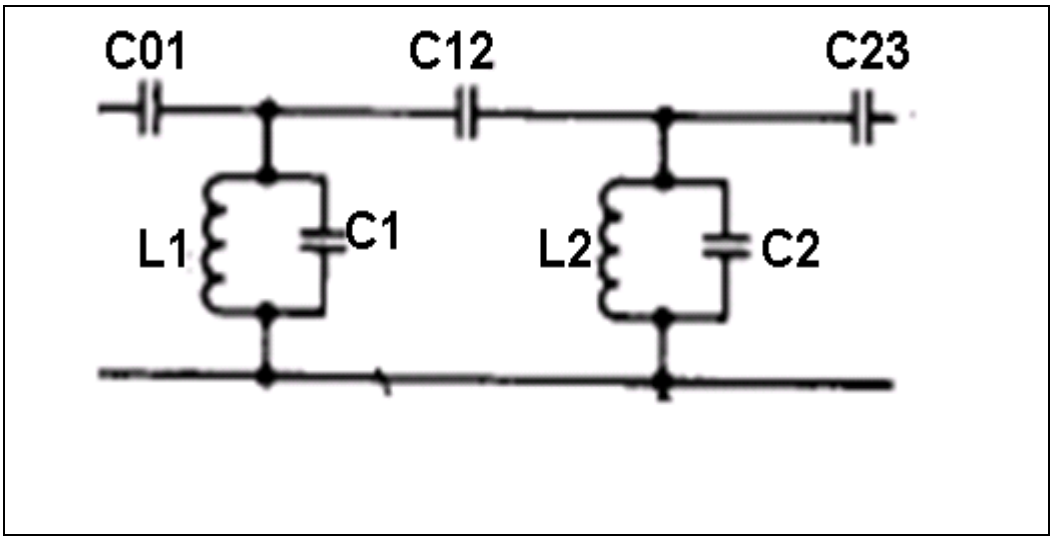


Figure 3.2 Coupled resonator filter

The Figure 3.2 shows a second order coupled resonator filter implemented with lumped inductors and capacitors. This bandpass filter is first implemented in its low pass form and then transformed to the band pass counterpart using frequency transformations. The design equations of the filter are followed from [32]. The filter basically consists of 2 parallel LC tank circuits which are designed to a desired resonant frequency. These two tank circuits are coupled using a center coupling capacitor C12. The matching capacitors C01 and C23 are provided to give a 50 ohm match so that the filter can be interfaced to other components in the receiver.

3.2 Bandpass filter at 5GHz

A bandpass filter with a center frequency of 5 GHz and a 3dB bandwidth of 600 MHz was designed to demonstrate the use of the high Q inductors designed in chapter 3. Such a bandpass filter can be used for WLAN applications. The bandpass filter was initially designed in Advanced Design System (ADS) which is a circuit simulator , in order to

determine the values for unloaded Q's for the inductors and capacitors required to implement the filter. Figure 3.3 shows the coupled resonator filter using ideal lumped elements with 50 ohm terminations. The return and insertion loss of this filter is shown in figures 3.5 and 3.6.

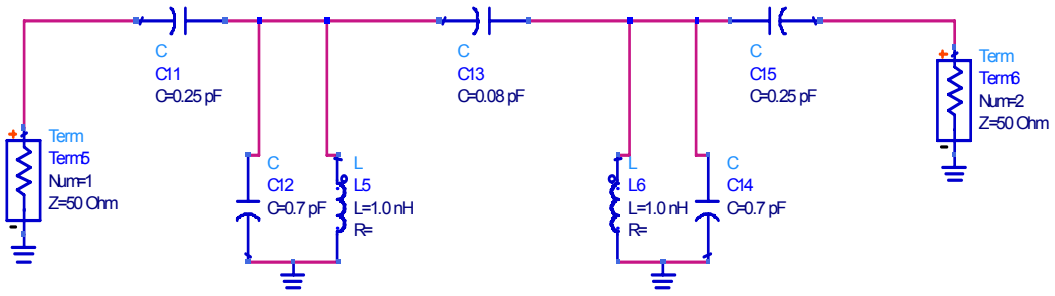


Figure 3.3 Band pass filter with ideal elements

The ideal filter gives an insertion loss of about -0.02 dB and a return loss of about -31 dB. However, this representation is not valid for practical purposes and hence another form of the same circuit is shown in figure 3.4. This circuit uses the lossy lumped elements. The loss is implemented in terms of the quality factor of the inductor and capacitor which is shown highlighted in the figure. It was seen that a quality factor of about 100 at 5GHz is required for the inductors while a quality factor of about 50 is needed for the matching and coupling capacitors. These are the requirements on the unloaded Q in order to get an insertion loss and return loss of about -4dB and -23dB respectively along with acceptable roll off at 600 MHz bandwidth.

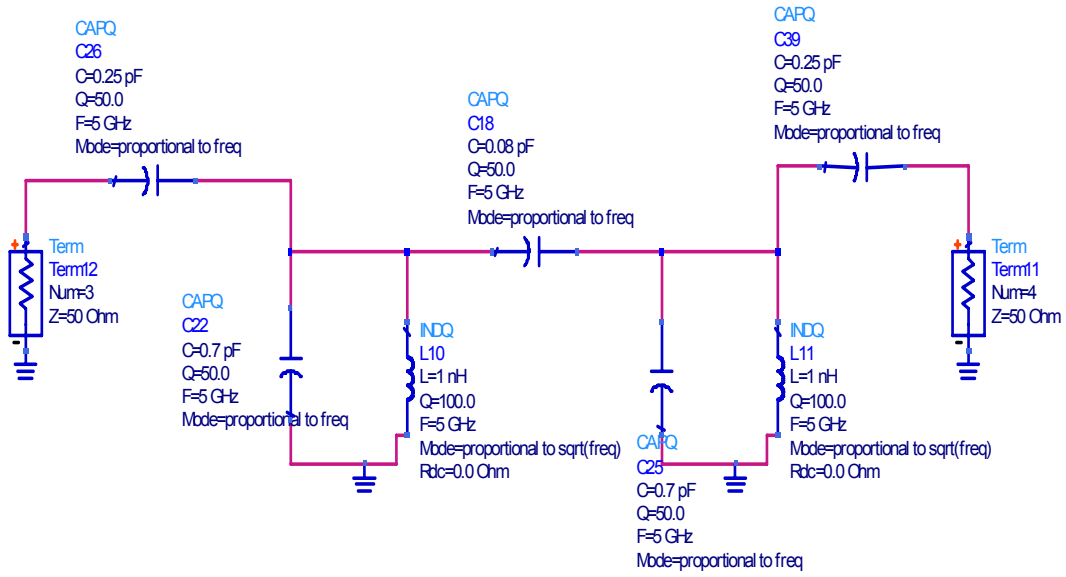


Figure 3.4 Bandpass filter with lumped elements with realistic Q values

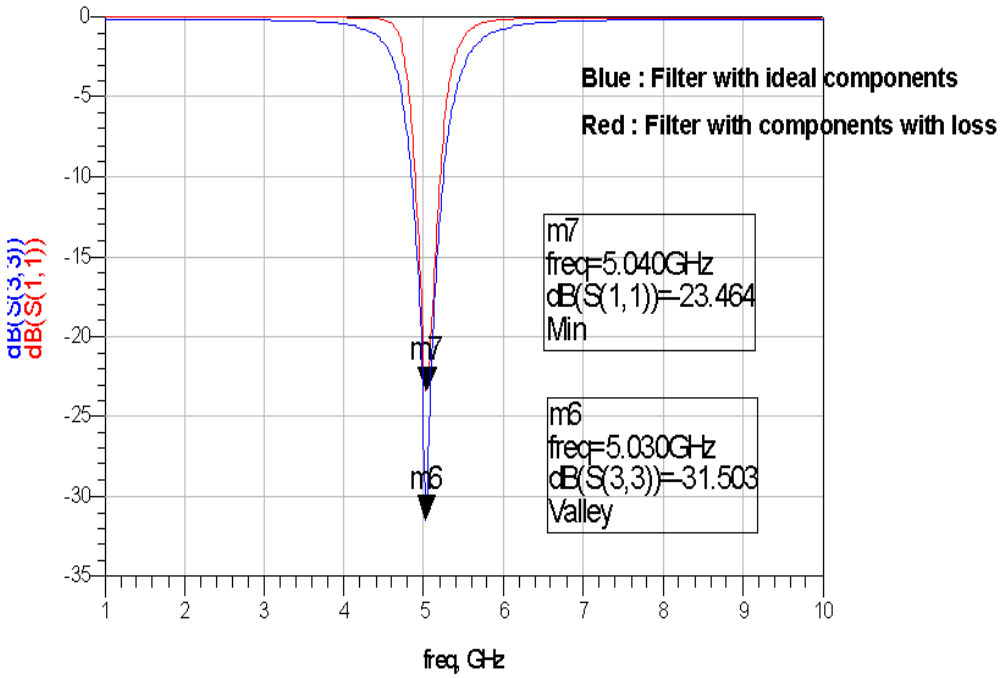


Figure 3.5 Insertion loss of the ideal and practical filter

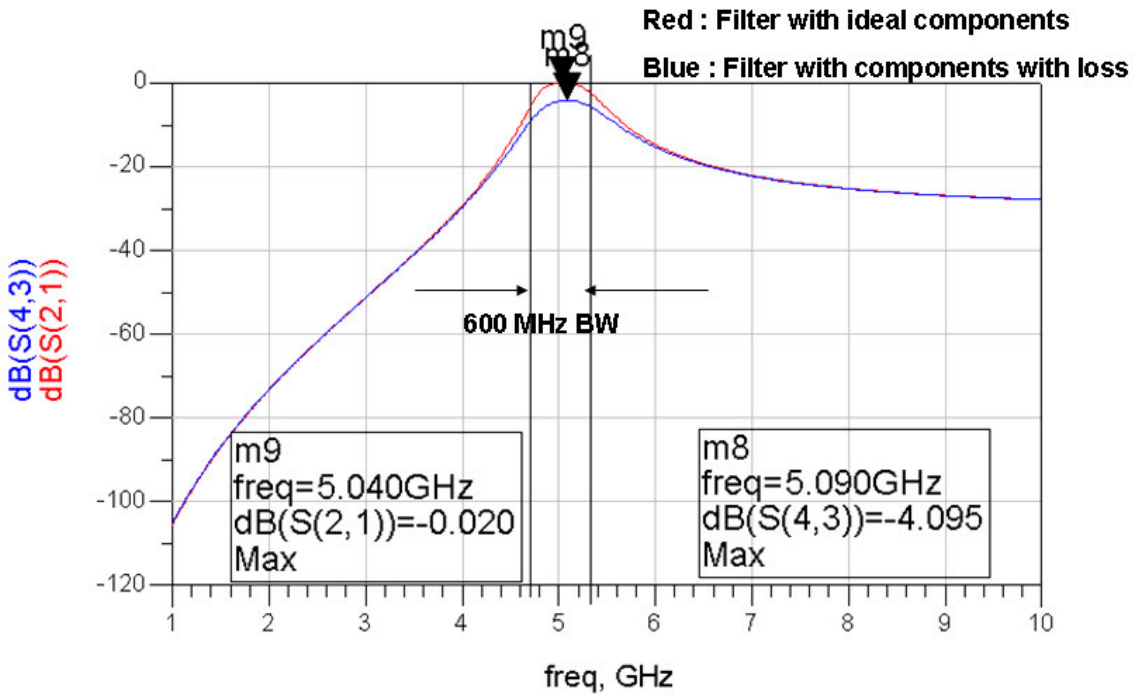


Figure 3.6 return loss of the ideal and practical filter

This filter was designed on both TV1 and TV2. The filters were designed using an electromagnetic simulation tool – SONNET. For the filter designs on TV1, the center coupling capacitor and the matching capacitors are interdigital capacitors while the capacitor which forma part of the parallel resonator is implemented as a parallel plate capacitor. A ¾ turn inductor was used in the parallel tank circuit. The components were designed individually in SONNET to achieve the required unloaded Q's. Figure 3.7 shows the design as in SONNET along with the GSG probe pads. The 3D view of the filter is shown in Figure 3.8.

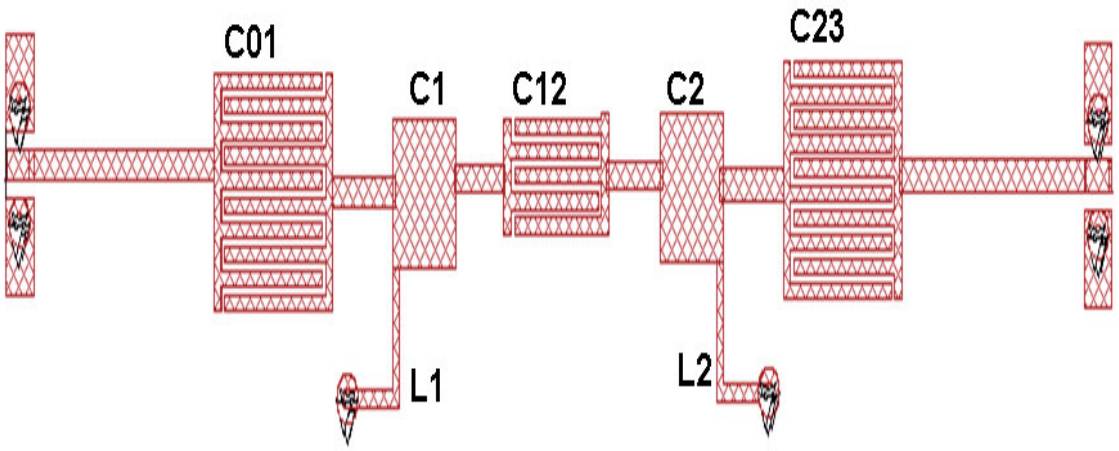


Figure 3.7 SONNET model of BPF on TV1

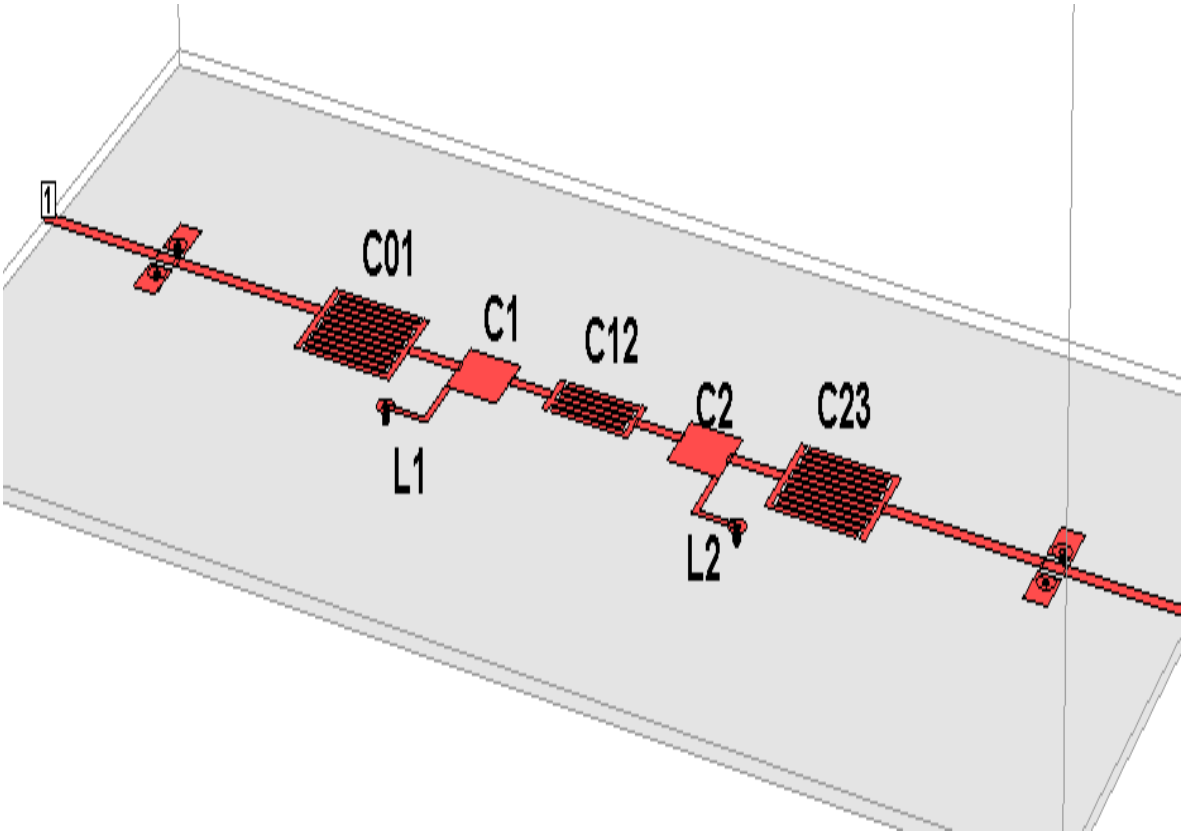


Figure 3.8 3D model of the BPF on TV1

The response of the filter designed on TV1 is shown in Figure 3.9

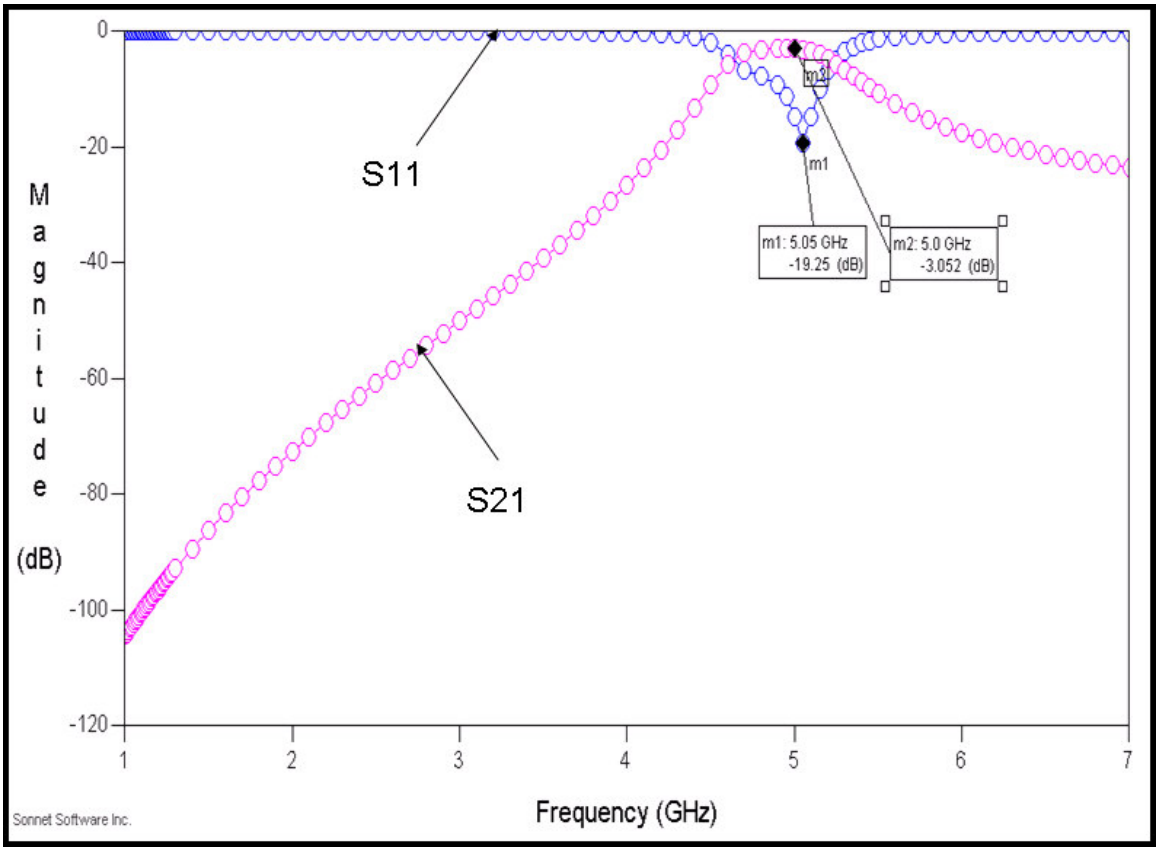


Figure 3.9 Insertion and return loss

The filter was designed on TV2 using 2D and 3D parallel plate capacitors and spiral inductors. The 3D capacitors exploited the availability of 4 metal layers and helped to achieve the capacitance required in a smaller area and volume. Figure 3.10 shows the SONNET model of the filter. The filter occupied an area of about 1.6mm x 2.6 mm. Capacitors C1 and C2 were implemented as 3 D capacitors as shown in Figure 3.12.

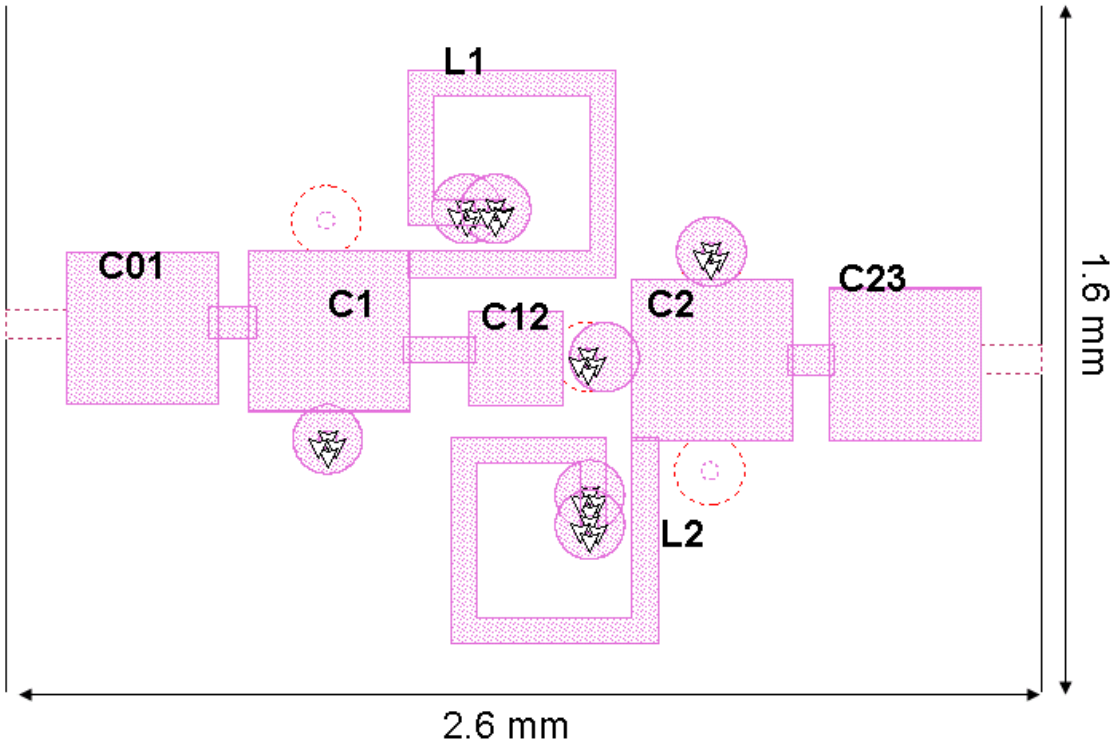


Figure 3.10 SONNET model of BPF on TV2

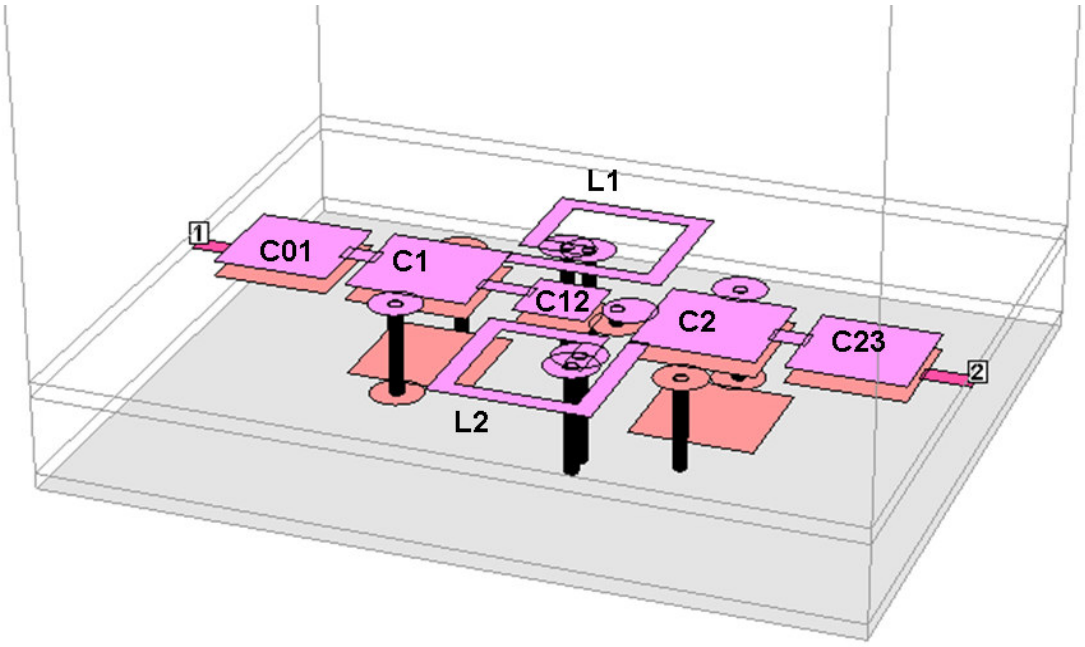


Figure 3.11 3D model of the BPF on TV2

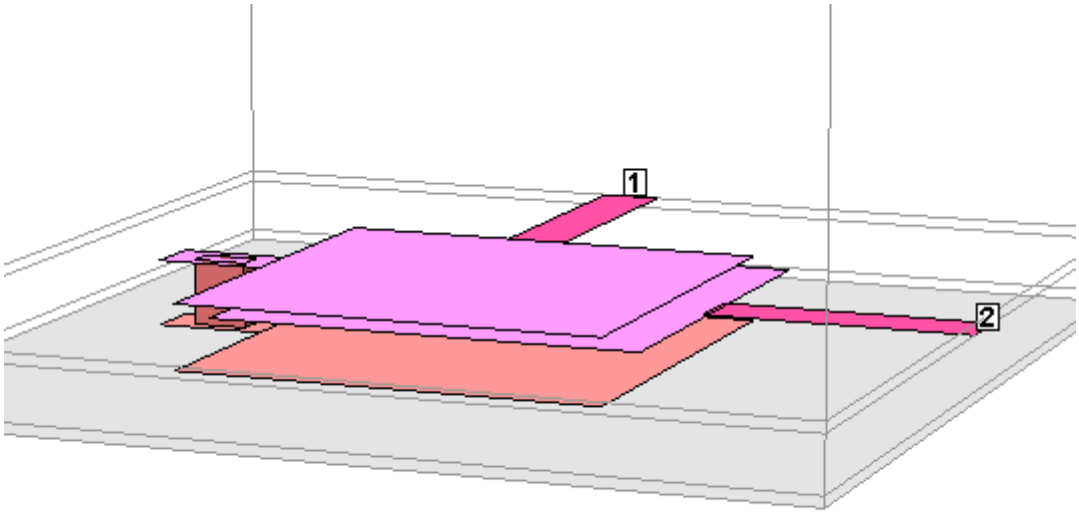


Figure 3.12 3D capacitor

The response of the TV2 filter is shown in Figure 3.13.

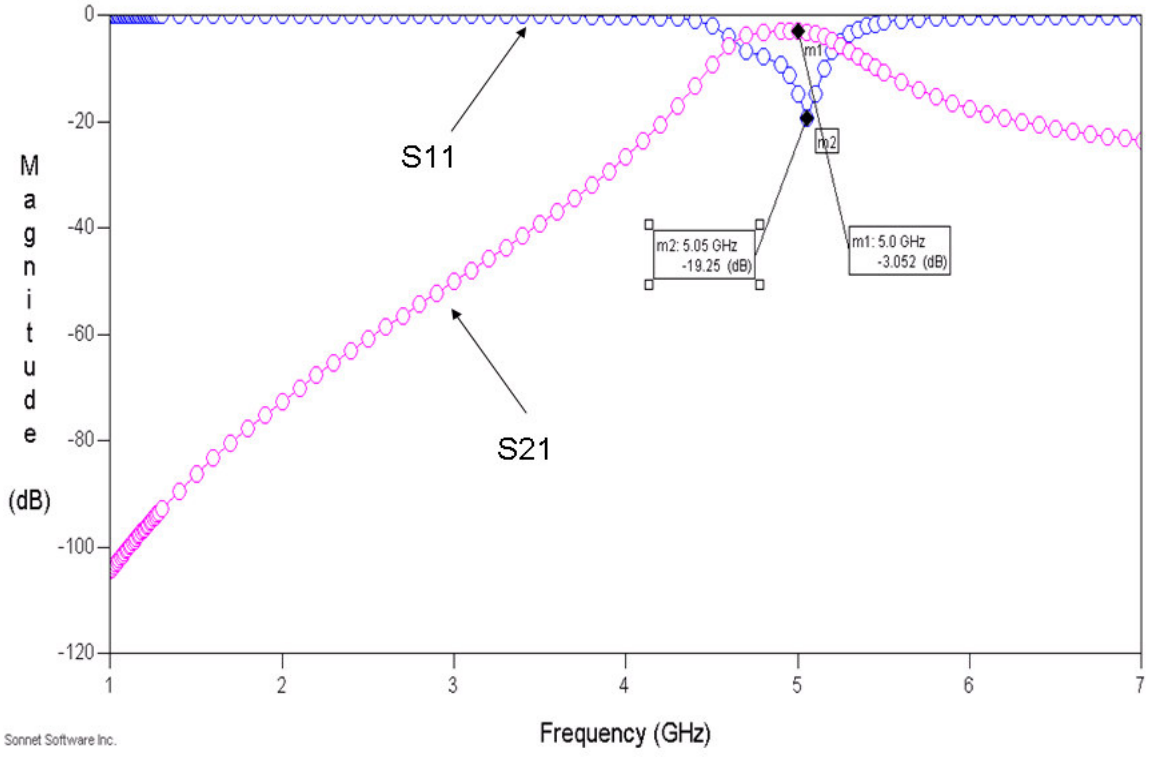


Figure 3.13 Insertion and return loss

3.3 TV1 Filter test vehicle

The filters were built as part of a larger test vehicle consisting of other filters designed between 2 – 3 GHz. The test vehicle measured 6 inches x 6 inches. It has four coupons distributed around the area of the board. Each coupon consisted of four filters . The test vehicle was fabricated using the standard organic laminate process described in the last chapter. A picture of the fabricated filter is as shown in figure x and the fabricated test vehicle is shown in Figure 3.14

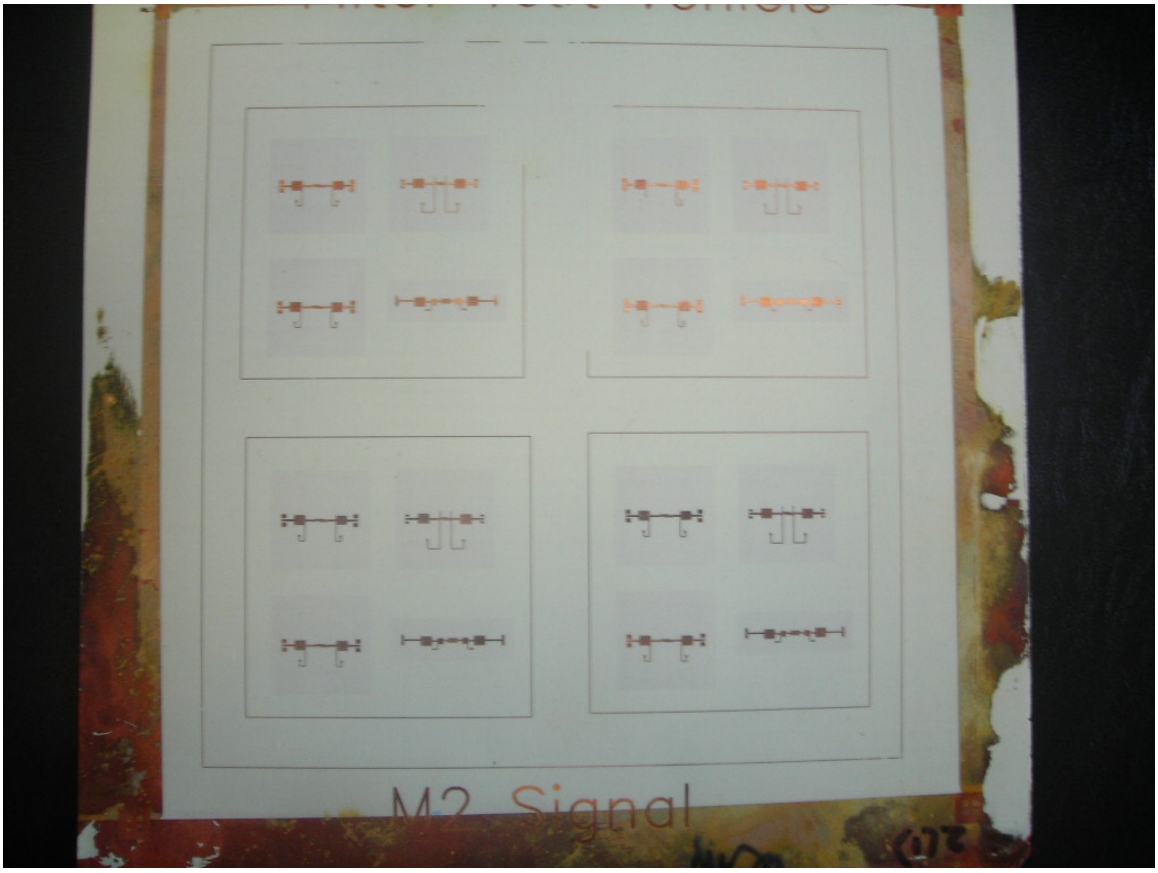


Figure 3.14 Fabricated filter test vehicle

3.4 Measurements

2 port Vector Network Analyzer measurements were done on TV1 with 500 um GSG probes using SOLT calibration. The characteristic impedance was 50 ohms and hence no de – embedding is required. A comparison of the measured to modeled results is shown in Figures 3.15 and 3.16

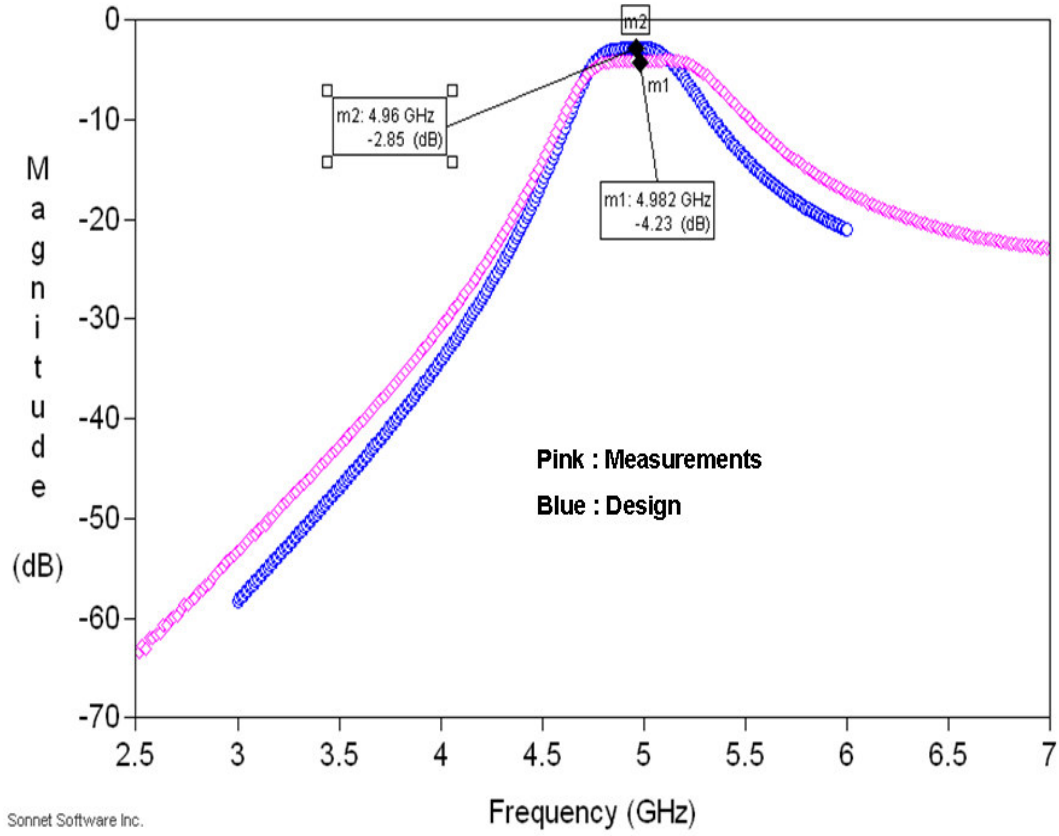


Figure 3.15 Measurement results for insertion loss

Figure 3.15 shows the insertion loss and fig 3.16 shows the return loss. There is a difference of about -2 dB between the designed and measurement results in the insertion loss and a considerable difference in the return loss. This difference may be attributed due to the fabrication inconsistencies. Table 3.1 shows the comparison between designed

and fabricated dimensions for the filter

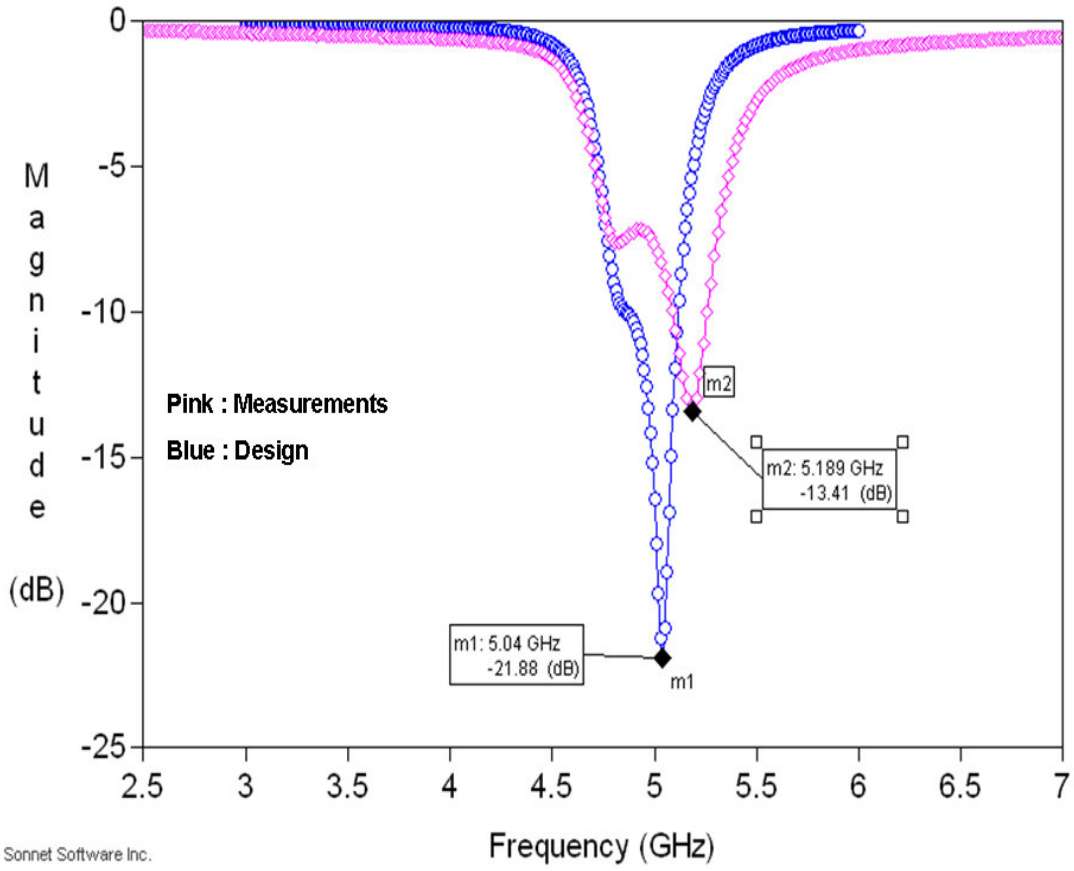


Figure 3.16 Measurement results for return loss

Table 3.1. Measured vs Designed Dimensions of filter

Parameter	Measured	Designed	% Variation
W2	93	100	7.5
S2	56	50	10
W4	95	100	5.3
S4	54	50	7.4
W6	94	100	6.4
S6	54	50	7.4
W8	85	100	17.6

Table 3.1 continued

W9	84	100	19
L1	875	890	1.7
L2	875	890	1.7
L3	875	890	1.7
L4	875	890	1.7
D1	280	300	7.2
D2	276	300	8.7

The dimensions are marked as shown in figure 3.17.

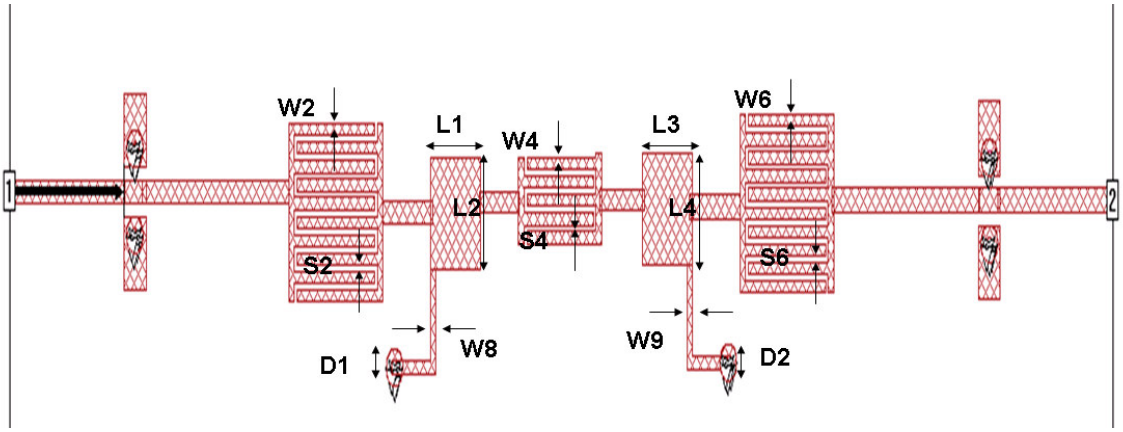


Figure 3.17 Measured Dimensions

These dimensions were plugged back into the model and the resulting comparison for the insertion loss is shown in figure 3.18.

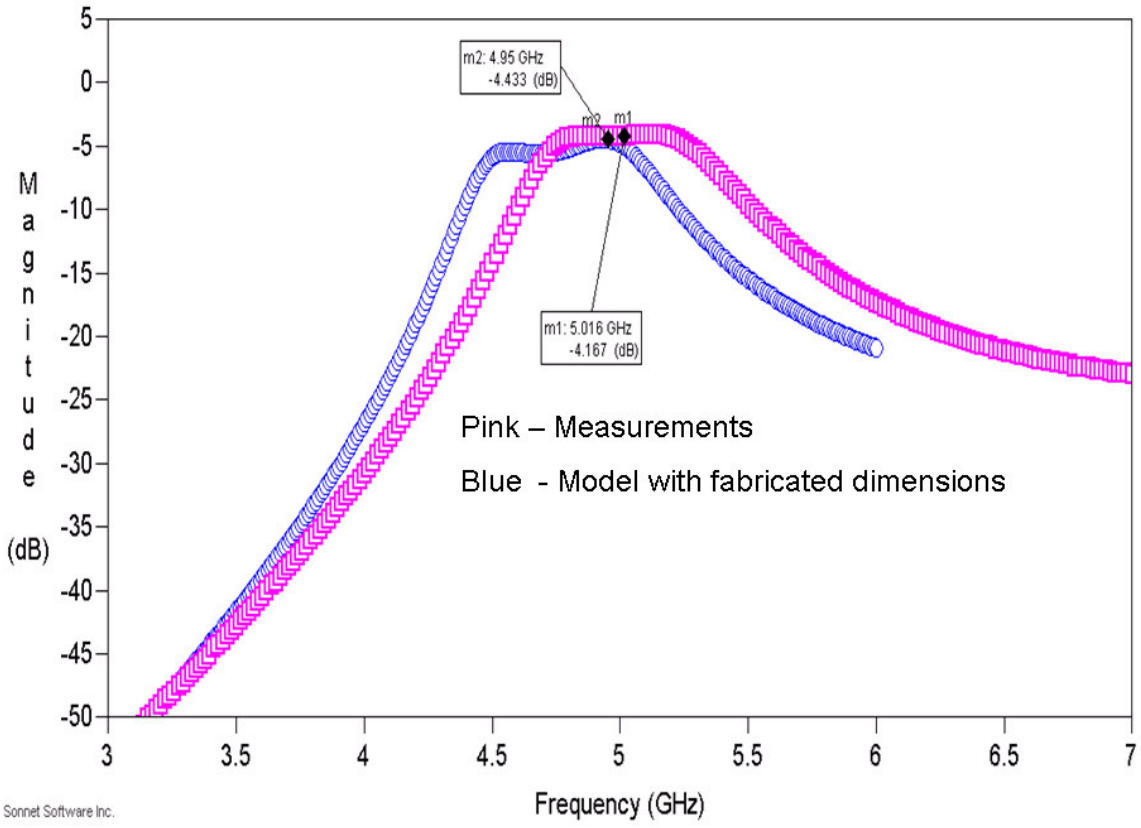


Figure 3.18 Insertion loss comparisons between fabricated and designed dimensions

As shown in figure 3.18, there is a difference of about 0.3 dB in the insertion loss between the measured and the modeled results (new fabricated dimensions). This shows that by improving the fabrication process, the designs can be made to coincide with the fabricated results. The main problems faced with the current fabrication process were the lack of metal thickness control during plating and the in efficient control of etching rate which is related to the metal thickness. By controlling these two factors, better filters can be fabricated.

3.5 Conclusion

Proof of concept demonstration of filters is shown in this chapter. Simulation results for bandpass filters at 2.4 GHz and 5 GHz is shown on the two test vehicles – TV1 and TV2. Measurements results are shown for the BPF at 5GHz and good correlation is demonstrated between modeled and measured results. An insertion loss of about -4dB is measured at 5GHz and the filter has a 3dB bandwidth of about 600 MHz.

CHAPTER 4

CONCLUSION

Compact size, faster time to market and cost reduction make the system on package approach an effective solution to RF front end packages. Multiband system architecture SOP is very important. It provides functionality in the package through the integration of passives such as inductors, capacitors and resistors. One of the key technologies for higher integration in SOP's is embedded passives technology. High Q passives embedded in the substrate enable high performance with compact size.

Of all the RF passives, inductors play a crucial role in determining the system performance of important components such as front end filters, BALUN's and VCO's. It is important to design inductors with high unloaded Q's in the desired frequency range to ensure enhanced performance of these entities. The other factor to be taken into account is the ground separation required for achieving this value of unloaded Q. Typically, at radio frequencies, the ground separation required is about > 800 microns. This value prevents the miniaturization of the RF packages.

The current research has provided a solution to this problem by demonstrating high Q RF inductors in the frequency range of 1 – 20 GHz with a reduced ground separation of about 100 – 140 microns. New designs have been implemented on a new family of low loss organic substrates. Two test vehicles have been designed, fabricated and measured and characterization data has been provided. This work has demonstrated unloaded Q's or RF inductors in the range of 70 – 200. The effectiveness of the work has been done by the introduction of a new metric – volume density of the inductors. The concept of

miniaturization has been brought into the design domain by this metric. The current work has demonstrated high Q inductors in volumes of the order of $0.07mm^3$ which is more than an order smaller when compared to the inductors demonstrated on LTCC and organic substrates. This reduction in volume is the result of reduced lateral area occupied along with the reduction in thickness contributed by the thin substrates. This dissertation has also demonstrated RF front end filters using the designed low profile inductors to show a proof of concept demonstration.

Thus, the current work is an attempt to show high Q RF inductor designs possessing the best attributes of Silicon (reduced area) and LTCC / Organic (high Q's) , that occupy very low volumes.

4.1 Future Work

The work presented in this thesis can be extended to study and analyze the influence of the high Q inductors on RF circuits such as Voltage Control Oscillators (VCO's) and BALUNs. The reason behind this future approach is to study the effect on active devices and to look at the total miniaturization. Fabrication and measurements of inductors on the four metal layer is also part of the future work. There is also a need for evaluating the effect of changes in temperature and time on the quality factor, inductance and insertion loss of the inductors and filters respectively. Apart from this a study of the effect of a real package (with metal planes surrounding the inductor) on the inductor performance also needs to be done.

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